September/October 2001 - Advancing Microelectronics   27

IMAPS 2001 Technical Program

Tuesday
October 9, 2001

TA1
MEMS in Aerospace and Aeronautics Applications
Session Chair: John Champion, The Johns Hopkins University/APL
10:10 am - 11:50 am

The utilization of MEMS enables a reduction of mass, volume, and electrical power, offering the opportunity for numerous solutions in space applications. The requirements for reductions in mass and volume are currently seen in the movements toward nano and pico satellites. Examples of how MEMS help in accomplishing these goals are given in the session papers.

Overview on CMOS MEMS Fabrication Techniques and Applications
Michael Gaitan, NIST

MEMS in Aerospace Applications - Thermal Control Shutters
R. Ostander, J. L. Champion, M. A. Darrin, The Johns Hopkins University/APL

MEMS in Space Science
Rainer K. Fettig, NASA Goddard Space Flight Center/Raytheon ITSS

Micro-Scale Avionics Thermal Management
Matthew E. Moran, NASA Glenn Research Center

TA2
Next Generation Manufacturing Technology
Session Chairs: Nicole L. Cavanah, Rockwell; Terry Baum, CTS RF Integrated Modules
10:10 am - 11:25 am

This session encompasses new developments in materials and processes. Developments in materials and processes are constantly pursued to meet customer requirements of cost, reliability, and size. The papers in this session will highlight new developments in wirebonding, LTCC, and advanced materials.

Zero Shrink Process for Cost Sensitive High Volume LTCC Applications
Mike F. Barker, Rick Draudt, DuPont Microcircuit Materials

Evaluation of Advanced Materials to Satisfy Higher Reflow and Solder Joint Life Requirements on MAP BGA
Mark Gerber, Trent Thompson, Shawn O’Connor, Motorola Semiconductor Products Sector

TA3
Microfabrication
Session Chair: Jay Jayaraj, Foster-Miller
10:10 am - 11:25 am

Increases in packaging density come from and through advances in density of all types of interconnections. This session illustrates several areas in which interconnect density enable performance or application improvements.

Fabrication and Assembly of a Digital Transducer-to-Bus Interface Module having a Directly Attached MEMS Device
Namsoo P. Kim, Nelli Amirgulyan, Kin Li, Chung-Ping Chien, Minas H. Tanielian, The Boeing Company

Development of an Organic Micromachining Process on Silicon for RF/Microwave Applications
D. Neulin, A. Pham, J. Harriss, Clemson University; J. B. Lee, University of Texas - Dallas

Large Suspended Bond-wire High Q Solenoid-type Inductors and SrTiO3 Thin Film Capacitors for Wireless Applications
Jae Y. Park, Yun S. Eo, Jong U. Bu, LG Electronics Institute of Technology; Kye I. Jeon, RF Core Co. Ltd.

TA4
HD Organic Board Technologies
Session Chair: R. Wayne Johnson, Auburn University
10:10 am - 11:50 am

Vias are a critical issue in high density laminate substrate technology. Microvias and blind vias are two approaches to achieving higher routing densities. For laminate substrates used in packages, the solder mask is an integral layer between the laminate and the molding compound. Solder mask strength and crack resistance is important for package reliability. For flip chip assembly in the package, either the die is bumped or as described in the last paper, the bump can be fabricated as part of the PWB.

Moving to Microvias in a High Reliability, Low Production Environment
John Folkerts, Paul Falk, Anne Dietrich, Binb Le, Sharon Ling, The Johns Hopkins University/APL

Accuracy Enhancement of Blind via Depth-Controlled Drilling
Christian P. Williams, The Johns Hopkins University/APL

Strength Evaluation of Microelectronics Packaging Solder Mask Materials
Maurice Othieno, Manickam Thavarajab, Patrick Varioi, Ranganathan Ramaswamy, LSI Logic Corporation; Jayamalar Vijayen, San Jose State University

High Density Wiring Substrate with Molded Polymer-Core Bumps for Flip Chip CSP
Nidori Kobayashi, Yasuakazu Kishimoto, Toshiba Chemical Corporation; Kazubito Higuchi, Susumu Kimijima, Toshiba Corporation
**TP1**
Recent Development in Wafer Level Chip Scale Packages

Session Chairs: Beth Keser, Motorola Inc.; Michael Toepper, Fraunhofer IZM

2 pm - 5:25 pm

Wafer level CSP technologies are the fastest growing class of packaging technology currently in development. This rapid proliferation is being fueled by the need for package size minimization in a host of portable computing and communication products. This session addresses advancements that are being made in WL CSP process technologies which are aimed at cost effective minimal packaging with the improved board level reliability.

A Polymer Reinforced WLP / Why it has Superior Solder Joint Reliability
Deok-Hoon Kim, Peter Elenius, Scott Barrett, Kulicke & Sojka - Flip Chip Division

Assembly and Reliability of a Wafer Level CSP
Parvez M. Patel, Motorola; Anthony Primavera, Universal Instruments Corporation; K. Sribari, State University of New York - Binghamton

Stencil Printing Process of Buffer Layer for Wafer Level CSP
Hirokazu Ezawa, Masaharu Seto, Masabiro Miyata, Hiroshi Tazawa, Toshiba Semiconductor Company

On-Wafer Process for Stress-Free Area Array Floating Pads
Raymond A. Fillion, Robert J. Wojnarowski, Herbert Cole, Glenn Claydon, GE Corporate R&D

Indium Bump Bonding for Cryogenic Applications
Allen C. Keeney, David M. Lee, S. John Lehtonen, A. Shaun Francomacaro, Johns Hopkins University/AIPL

Low Cost Solder Bumping via Paste Reflow for Area Array Packages
Benlibi Huang, Ning-Cheung Lee, Indium Corporation of America

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**TP2**
Wideband Materials Characterization for RF, Microwaves, and Wireless

Session Chairs: Michael Stein, Electro-Science Labs, Inc.; Peter Barnwell, Heraeus Inc., Circuit Materials Division

2 pm - 5:25 pm

The session deals with materials issues for both radio and microwave frequencies of the spectrum, with emphasis on lead-free, low-loss dielectrics, and photo patterned conductors compatible with low temperature cofired ceramic systems. RF & Microwave design and packaging engineers need vital the acquisition of essential electrical high frequency data on various advanced electronic materials properties to serve various basic functions including interconnects. These materials data and information mainly include the complex dielectric constant, the material conductivity, and the attenuation component. The challenging design mandates additionally electronic products possessing specific desired electrical attributes, while still meeting basic thermal and mechanical essential requirements with high reliability and high yield.

Higher K Low Loss Dielectric Ceramic Co-fired with a Commercial LTCC Tape System
Weiming Zhang, J. Thomas Hochbeimer, Christina Modes, Peter Barnwell, Heraeus Inc., Circuit Materials Division; Steve Dai, Motorola Labs.

Lead Free Dielectric Tape System for High Frequency Applications
A.H. Feingold, R.L. Wablers, S.J. Stein, Electro-Science Laboratories

RF Characterisation of No-Clean Solder Flux Residues
Maeve Duffy, Paul McCloskey, PEI Technologies; Liam Floyd, Cian Ó Mathbáin, NMRC; Karen Telffensen, Mike Liberatore, A. Sreeram, Alpha Metals-USA

Self Adhesive Metallization (SAM) - A New Concept in LTCC Technology
Liang Chai, Aziz Shaikh, Vern Stygar, Ferro Electronic Materials

Photo Patterned Conductors with LTCC for Microwave and High Density Interconnect
Peter Barnwell, Brent Smitb, Heraeus Inc., Circuit Materials Division; Michael Ebler, National Semiconductor Corporation

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**TP3**
Materials

Session Chairs: Herb Neuhaus, NanoPierce Technologies; Susan Bagen, Advanced Process Concepts

2 pm - 5:25 pm

Advances in materials are the key to microelectronics packaging. The papers in this session describe a number of advances in materials used in interconnect technology, and cover both board and assembly levels.

Z-Axis Interconnection for 3-D High Density Packaging

Transparent Conducting Oxides Based on AghnO2 Delafossite
Jane E. Clayton, David P. Cann, Alan P. Cons tant, Iowa State University

Characterization of AlMgB14 Materials: An Ultra-Hard Material
T. L. Lewis, A. Russell, B. Cook, J. Harringa, Iowa State University

Pre-Applied Underfill Adhesives for Flip Chip Attachment
Scott Charles, Michael Kropp, Robert Kinney, Steve Hackett, Robert Zener, Fuming (Bruce) Li, Roger Mader, Peter Hogerton, 3M Company; Arun Chaudhuri, Frank Stepiak, Matthew Walsh, Delphi Automotive Systems

CSP Flux-Free Underfill Resin for Electrical Connection and Physical Adhesion Material, Process and Technology
Kenji Kitamura, Toomoaki Nemoto, Sbotchi Fujimori, Naoki Kanagawa, Shinji Hashimoto, Taro Fukui, Matsushita Electric Works, Ltd.
Characterization of Ruthenia-Based Resistors Embedded in Low Temperature Co-fired Ceramic Substrates
Sben-Li Fu, Chi-Shiung Hsi, I-Shou University

Screen-Printed Pb(Zr, Ti)O3 Thick Films for Ultrasonic Medical Imaging Applications
Marija Kosec, Janez Holc, Joze Stefan Institute; Franck Levassort, Louis Pascal Tran-Huu-Hue, Marc Letbiecq, LUSSI/GIP Ultrasons

TP4 Thermal Management
Session Chairs: Ajay P. Malshe, University of Arkansas; Tarak Railkar, Conexant
2 pm - 5:25 pm

Demands and advances in the thermal management area are highlighted in this session through various presentations by leading researchers on topics such as miniaturized heat pipes, reliability of high power optical devices, analysis and modeling.

Synthetic Jet Based Active Heat Sink for Electronic Cooling
Raghav Mahaligam, Ari Glezer, Georgia Institute of Technology

Operation Performance of Miniature Heat Pipe with Composite Wire Wick
Seok Huan Moon, Ho Gyeong Yun, Gunn Huang, Tae Goo Choi, ETRI

Failure Mechanisms in High Power Optical Device Packaging: Semiconductor Laser Diodes - A Case Study
Ajit R. Dhamdhere, Ajay P. Malshe, S. N. Yedave, W. F. Schmidt, W. D. Brown, University of Arkansas (HiDEC-MEEG); John Morales, Coherent Semiconductor Inc.

Numerical and Experimental Simulation of Electro-Thermal Behavior of VLSI Chips

Thermal Design of Desktop Server Switch with Detailed Modeling of High Power TBGA Packages
S. Z. Zbao, Broadcom Corporation

TP5 High Density Packaging
Session Chairs: Rajen Chancbani, Sandia National Laboratories; Scott Popelar, IC Interconnect
2 pm - 5:25 pm

In this session, several advanced, high density substrate and MCM technologies will be presented. The first two papers report a new way to process organic laminate substrate and the photoinitable low temperature co-fired ceramic substrates, with fine features. A new 3D packaging technology with embedded active and passive devices will also be presented. Next, several papers also report MCM-D technology with variety of base substrate materials.

A New High Density Organic Laminate
Katsuna Hayashi, Teruya Fujisaki, Masaaki Hori, Kyocera Corporation

Novel Ceramic Packages and Architectures for MST Applications made possible with Photoinitable LTCC
Barry E. Taylor, Larry Bidwell, Angela Lawrence, Tim Mobley, Daniel L. Aney, DuPont Octronics

High-Density Multi-Layer Thin-Film Packaging Technology for High-Performance ASIC Chips
Katsumi Kikuchi, Tadanori Shimoto, Hirokazu Honda, Keiichiro Kata, Koji Matsui, Sueo Morishige, NEC Corporation

A New 3-D Module using Embedded Actives and Passives
Y. Sugaya, T. Asabi, S. Komatsu, Y. Yamamoto, T. Ogawa, S. Nakatani, Matsushita Electric Industrial Co., Ltd.

A Multi-Layer Thin-Film MCM-D QPSK Modulator for VSAT Applications

The PSGA, A Lead-Free CSP for High Performance & High Reliable Packaging
Barbara Vandeveld, Arun Chandraokes, Evelien Driessens, Eric Beyne, IMEC; Jef Van Puyenbroeck, Marcel Heerman, Siemens

The Challenge of Overcoming Wire Sweep in Ultra-Fine-Pitch Wire Bonded Ball Grid Array Packages
Robert Radke, Lois Yong, Tu-Anh Tran, Motorola; Fuaida Harun, Ruzaini Ibrabim, Motorola Malaysia Sdn. Bhd.

TP6 National Science Foundation and IMAPS Educational Foundation
Session Chair: Rao Tummala, Georgia Institute of Technology

Microwave Characterization of Low Temperature Cofire Ceramics with Embedded Fluid Channels
Orfirio Sanchez, Florida International University

Electrically Conductive Adhesives Technology
James E. Morris, TJ Watson School of Engineering & Applied Science

Efficient and Economical Laser Processing of Mixed Signal Packaging
T. Darren Brown, University of Kentucky

Mechanisms of the Adhesion of Aromatic Thermosetting Copolyesters (ATSPs)/Si02 and ATSPs/Polyimides
Amir Alam, University of Illinois at Urbana - Champaign

WA1 High Density Packaging for Portable Terminal Equipment in Japan (Japanese Translated Session)
Session Chairs: Yuzo Shimada, NEC Corporation; Charles E. Bauer, TechLead Corporation
8 am - 10:55 am

The leaders in mobile electronics product and technology for more than 40 years,
Japan now leads again in the application of flip chip packaging techniques for today’s portable consumer products. This session presents current deployment alternatives for flip chip in Japanese products and demonstrates cost effective flip chip use in telecommunication appliances, personal computing devices and other mobile products.

**High Density Packaging using Flip Chip Technology in Mobile Communication Equipment**

Kazuto Nishida, Kazunichi Shimizu, Takashi Yui, Hajime Honma, Nobuya Matsumura, Matsushita Electric Industrial Co., Ltd.; Izumi Okamoto, Matsushita Electronic Components Co. Ltd.; Kouji Abe, Kouzou Takada, Tomiyo Ema, Matsushita Communication Industrial Co., Ltd.; Hideo Koguchi, Chie Sasaki, Nagaoka University of Technology

**Assembly Technology for Miniaturization of Mobile Terminals**

Tadao Otani, Yoichiro Maehara, Satoru Hara, Miki Mori, Takashi Koyanagawa, Mitsuharu Yamabe, Toshiba Corporation

**LTCC Module using Flip-Chip Technology for Mobile Equipment**

Jitsubo Hirota, Tatsuya Funaki, Akibiro Miwa, Murata Manufacturing Co., Ltd.

**The Technology of Flip Chip Bonding on an Organic Substrate for PDA**

Akira Makabe, Yobei Kurashima, Satoshi Shimizu, Shigeki Inoue, SEIKO EPSON Corporation

**Packaging Technology for Mobile PCs**

Shunichi Kikuchi, Kiyokazu Morizumi, Kazubisa Tsunoi, Takumi Kishi, Fujitsu Limited

**Sn-Zn Lead-Free Solder Applied to Notebook Personal Computer**

Motoji Suzuki, Hiroshi Matsuoka, Eiichi Kono, Makoto Igarashi, NEC Corporation

**WA2 Integrated Passives in LTCC for RF, Microwaves and Wireless**

Session Chairs: John Gipprich, Northrop-Grumman; Fred Barlow, University of Arkansas

8 am - 11:20 am

The session deals with integrated passives in low temperature cofired ceramic systems. Thermal management is a crucial issue to be addressed in the LTCC manufacturing process, as a potential emerging technology for telecommunications, including instrumentation, military, space, satellite communications, adaptive antennas, data and wireless transmission, directions finder, radar, electronic counter measures, threshold detection, local area networks, cellular & personal communications services (PCS), GPS, ISM, and wireless market driven products in general. Components and break through trends in passives integration, advanced devices, and elaborate systems.
evolve as the drive mandates higher circuit densities and realization of finer pitch patterns (reducing device junction temperature and improving the thermal resistance of the various interfaces of the planar electronic materials).

Parameterized Libraries of Embedded Inductors and Capacitors in LTCC
R. Ramprasad, Feng Ling, William Blood, Thomas Myers, Michael Petras, Mel Miller, Motorola, Inc.

A Packaged Miniature Antenna for Wireless Networking
Bedri A. Cotiner, I. Jofre, F. De Flaviis, University of California - Irvine

Efficient Band Pass Filter Design for a 25 GHz LTCC Multichip Module using Hybrid Optimization
W. Simon, R. Kulke, A. Lauer, M. Rittweger, P. Waldow, I. Wolff, IMST GmbH

Power Distribution Networks in Multilayer LTCC for Microwaves

Design and Fabrication of Embedded Resistors in LTCC for High Frequency Applications
Gangqiang Wang, Venkat Rajagopalan, Fred D. Barlow, A. Elsbabini, W. Brown, Simon S. Ang, University of Arkansas

Glass-Ceramic Module for 60GHz-Band Wireless Communication Systems
Kazuhiko Ikuina, Takeya Hashiguchi, NEC Corporation; Kenichi Maruhashi, Masa-haru Itoh, Keicih Obata, Photonic and Wireless Devices Research Laboratories

In Situ Ultrasonic Stress Microsensor for Second Bond Characterization
Juergen Schweizer, Oliver Brand, Henry Baltes, ETH Zurich; Michael Mayer, ESEC

Wire Bond Temperature Sensor
Shtivesh Saman, Yogendra Joshi, University of Maryland; Michael Galatin, George Harman, NIST

High-Frequency Wirebonding: Its Impact on Bonding Machines

The Influence of Surface Defect Size on the Wire Bond Pull Strength for Automotive Lead Frame Materials
Philip W. Lees, David W. M. Williams, Barry Njoes, Technical Materials, Inc.

Fine Pitch 2nd Bond Evaluation for PBGA Packages: Process Capability and Reliability Assessments
Tu Anh Tran, Burt Carpenter, Lois Yong, Greg Ridsdale, Dennis Kavenscrauf, Fuada Haran, Edwin George, Motorola Semiconductor Products Sector

Wire Loop Development for Advanced PBGA Packages with Multiple Rows of Bonding Fingers and Power-Ground Rings
William K. Sbu, Philips Semiconductor

WA4
Power Packaging
Session Chairs: Doug Hopkins, State University of New York; Dave Kellerman, Material Solutions® Corporation

8 am - 10:55 am

Higher power density packaging is being addressed on several technological levels. Materials and processes are being developed and applied in high power density packaging including Cubic Boron Nitride, a novel LTCC/silver metal structure, a new thermally conductive die attach material, and diamond/diamond like film materials. The papers present structures to promote power in RF, MCM and discrete MOSFETs.

High Thermal Conductivity Cubic Boron Nitride Thick Films
Peter J. Gielisse, Jason P. Tremblay, Florida State University; Halina Niculescu, Florida Agricultural and Mechanical University; Selin Acbatowicz, Malgorzata Jakubowska, Elsbieta Zwiekowska, Institute of Electronic Materials Technology; Leszek J. Golonka, Tomasz Zauada, Wroclaw University of Technology; Viktor B. Shipilo, Elena Shishonok, Ludmila M. Gameza, Institute of Solid State and Semiconductor Physics

Thick Silver Tape in Low Temperature Cofire Ceramic (LTCC) for Thermal Management
Peng Wang, W. Kinzy Jones, Yanqing Liu, Florida International University

Silicon Carbide Power Die Packaging in Diamond Substrate Multichip Power Module Applications
A. B. Lostetter, K. J. Olejniczak, A. P. Malshe, W. D. Brown, Aicha Elsbabini, University of Arkansas

Evaluation of Embedded Power Technology for IPEM Packaging Applications
Zhennian Liang, Fred C. Lee, J. D. van Wyk, G-Q. Lu, Virginia Tech

Hybrid Modules as an Alternative to Paralleled Discrete Devices
Robin L. Farruggia, Donald K. Morozowich, Powerex, Inc.

High Efficiency Microwave Power Amplifier: From the Lab to Industry
William Herbert Sims III, NASA - Marshall Space Flight Center

WP1
Reliability of Novel CSP Structures
Session Chairs: Ernie Vastary, Micro Systems Engineering Inc.; James Cook, Promex

2 pm - 5:25 pm

CSP technologies are key drivers to the industry's continuing need for form factor...
reduction and/or improved functional integration. These technologies must also be able to withstand the stresses that handheld products are often subjected to. This session will address a range of topics related to mechanical modeling or reliability testing of CSPs at the component and board level.

Fracture Strength Characterization and Failure Analysis of Silicon Dies

Reliability Design and Experimental Work for Mirror Image CSP Assembly
Dongji Xie, Sammy Yi, FLEXTRONICS

Reliability and Failure Mechanism of Chip Scale Package on Laminate Technology
Zsolt Illyesfalvi-Vitéz, Pál Németh, Péter Bojta, Budapest University of Technology and Economics

Reliability Evaluation of CSP Electronic Devices Package
Hideo Koguchi, Chie Sasakti, Nagaoka University of Technology; Kazuto Nisbida, Matsushita Electric Industrial Co., Ltd.

The Effect of Compound Properties to Three Dimension Packages

Design and Reliability Study of Wire-Bonded μBGA® Packages for High Performance DRAM Applications
Ilyas Mohammed, Sridhar Krishnan, Young-Gon Kim, Tessera Technologies, Inc.

WP2
Integrated Passive Technology with PWB & Thin Film Processing for RF and High Speed Applications

Session Chairs: Robert Heistand, AVX; Timothy Lenihan, Seldanabl
2 pm - 5:25 pm

Integrated passive technology is being driven by the RF/wireless and high speed signal integrity applications. This session focuses on technology being developed in the printed wiring board and thin film fabrication arenas. Common themes are the innovations to increase specific capacitance, or raise the Q of inductor elements available for integration. Papers are selected from academia, material suppliers and systems houses.

Thin Film Capacitors Embedded into High Density Printed Circuit Boards
Angus I. Kingon, Taeyun Kim, Paul Vilarinho, Jon-Paul Maria, North Carolina State University; Robert T. Crosswell, Motorola Advanced Technology Center

Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards
William Borland, John J. Felten, DuPont iTechnologies

Lead-free High K Dielectrics for Integral Capacitor using MOCVD
Tatsuo Ogawa, Abmet Erbil, Swapan K. Bhattacharya, Georgia Institute of Technology

The Effect of Miniaturization on Embedded Resistors in High Density Interconnecting Substrates
Daniel D. Brandler, Omega Technologies, Inc.

The Integration of RF Passives using Thin-Film Technology on High-Ohmic Si in combination with Thick-Film Interconnect
Joost van Beek, Marc van Delden, Andre Jansman, Arjen Boogaard, Anton Kemmeren, Philips Research; Nick Pulsford, Arnold ten Dekker, Philips Semiconductors

WP3
Cu Wirebond and Reliability
Session Chairs: Michael Sheaffer, K&S Packaging Materials Group; Roupen Keusseyan, DuPont
2 pm - 5:25 pm

Copper metallization (bond pads) and low K dielectrics represent the next challenge facing IC manufacturing. Advanced wire bonding techniques are required for interconnection. This session will address interconnection issues for copper metallized integrated circuits. Wire bond reliability in harshly stressed and corrosive environments will also be addressed.

Wire Bonding to Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks and Materials Considerations
George G. Harman, Christian E. Johnson, NIST

Research on Prevention of Corrosion at Au-Al Bonds
Takuo Shoji, Keishi Miyamoto, Isao Shimizu, Yasubide Obno, Kumamoto University

Evaluation of Wire Bond Stresses in Plastic Encapsulated Packages
Pankaj Mitbal, Delphi Delco Electronics Systems

Wirebonds for Munitions Applications: Effects of Dynamic Shock, Vibration, and Spin
S. J. Lebtonen, H. K. Charles, Jr., The Johns Hopkins University/APL; G. Katulka, L. Burke, Peter Muller, N. Hundley, M. Ridges, Army Research Laboratory

Back-End Assembly Solution to Bare Copper Bond Pad Wafers
Chu-Chung Lee, Bill Williams, L.C. Tan, Susan Downey, Peter Harper, Motorola; Fuaida Harun, C. C. Yong, Motorola - Malaysia
A Reliable Copper Wire Bond Interface for Microelectronic Packaging
Nicole Cavanah, Rockwell Collins

Differences Between Aluminum and Copper Water Metallization in the Water Saw Process for Thin BGA Packages
Mark Gerber, Daniel Cavasin, Noel Arguello, Motorola-SPS

WP4 Lead-Free Solders
Session Chairs: R. Wayne Johnson, Auburn University; Herb Neuba, NanoPierce Technologies

2 pm - 5:25 pm
The electronics industry is moving to lead free assembly for environmental and market driven reasons. Solder alloys, fluxes, processing equipment, mechanical properties, and reliability are all issues that must be addressed prior to the switch to lead-free assembly. It is a very complex undertaking and this session will examine some of the key points.

Selection of Sn-Ag-Cu Lead-Free Alloys
K. Suganuma, K.S. Kim, S. H. Hub, Osaka University

Solder Paste with Polymerizing Flux for Lead-Free Solder Alloy
Tsutomu Nishina, Kenji Okamoto, Fujitsu Electric Corporate Research and Development, Ltd.

Improvement of Wave Soldering Equipment for Lead-Free Solder

Solder Joint Reliability of BGA Package with Sn-Bi System Solder Balls
Toshiba Akamatsu, Yatsuo Yamagishi, Fujitsu Laboratories Ltd.; Kazuyuki Imamura, Osamu Yamaguchi, Masaharu Minamizawa, Fujitsu Limited

A New Electrical Surface Joining Technology for Flip Chip Application

Interactive Forum (Poster Session)
1 pm - 4 pm
OptoBGATM for 10 Gbps Data Link
Masabiro Kijima, Mitsuo Yamagisawawa, Hisayoshi Wada, Seigo Matsuzono, Yuji Kishida, Takahiro Matsubara, Kyocera Corporation

Study of a Laser Microwelding Process for Microelectronics and Packaging
Wei Han, Ryszard Przputniewicz, Worcester Polytechnic Institute

Reliability of Bumpless TAB Component: CSPs and Bare Dies, for Harsh Environment Applications
P. Courant, D. Lambert, D. Roze, Bull SA

Computational and Experimental Approach to Study of a Nanoindentation Process for MEMS
Cosme Furlang, Dariusz R. Przyputniewicz, Ryszard Przputniewicz, Worcester Polytechnic Institute

Compact Folded-Line RF Power Dividers
C. Lim, R. K. Seetanuri, V. K. Tripathi, A. Weishaar, Oregon State University

A Study of the Effect of Fabrication Parameter Variation on the Environmental Characteristics of Thick Film Strain Gauges Fabricated on Steel Substrates
Yulan Zheng, John Atkinson, Zhige Zhang, University of Southampton; Russ Sion, C-Cubed Limited

Inexpensive Process for Flip Chip Manufacturing
Karel Malysz, Ivan Szendiuch, Technical University of Brno

A New Thermally Conductive Die Attach Film with Low Stress and Excellent Reliability
Takashi Masuko, Hiroki Hayashi, Shinji Takeda, Hitachi Chemical Co., Ltd.; Junko Morikawa, Toshiba Hasimoto, Tokyo Institute of Technology

New Direct-Write Technology for Pad Redistribution on Individual Die
Michael T. Daigman, Scott A. Matheus, David N. Wells, Potomac Photonics, Inc.;

Daniel Anthony, Microelectronics Research Laboratory

Development of a Low Volume Flexible Flip Chip Process
Alan P. Boone, Rockwell Collins

Power Cycling and Structural Integrity Approach for Assessing Reliability Performance of Electronic Packaging
Bor Chen Hong, Tsorng-Dib Yuan, IBM Microelectronics Division

The New Microelectronic Ignition Circuits for Sodium and Metal Halide Lamps
J. Gondek, K. Dzialek, Private Institute of Electronic Engineering; J. Kocol, B. Kawa, Technical School of Telecommunication; M. Ciez, W. Zaraska, R&D Centre for Hybrid Microelectronics and Resistors

85oC/85%RH or 40oC/95%RH? Contradictory Results in Climatic Reliability Tests
Gabor Harsanyi, P. Bojta, P. Nemeth, Budapest University of Technology and Economics

Radiation Tolerant Computer Solution for Space Environment
Anthony S. Lat, Steve Motter, Brian Dietz, Allegh Space Systems Inc.

Alternative Underfill Material for CSP Packages: Low Outgassing and Ionics Epoxy
Michael Ko, 3M Company; Chin Teong Ong, 3M Company - Singapore

Thursday
October 11, 2001

THA1 Flip Chip
Session Chairs: Andrew Strandjord, IC Interconnect; Phillip Garrou, Dow Chemical

8 am - 11:20 am
This session will be led by a survey of new flip chip applications and markets. New flip chip bumping technologies, lead-
Flip Chip Market Trends

A Compatibility Evaluation of Lead-Based and Lead-Free Solder Alloys in Conjunction with Electroless Nickel/Immersion Gold Flip Chip UBM
Scott Popelar, Andrew Strandjord, Bob Nieten, IC Interconnect

Lead-Free Solder Bump Technologies for Flip-Chip Packaging Applications
Zabeed S. Karim, Advanced Interconnect Teconology Ltd.; Rob Scbetty, Shipley LLC

Study of Underfill Resin Properties for High Performance Flip-Chip BGA Package
Yuko Sawada, Kozo Harada, Hirofumi Fujioka, Mitsubishi Electric Corporation

Novel Alignment Technologies for Wafer Level Packaging

Flip Chip Joining of Thin Chips on Flexible PEN Substrates
Erja Jokinen, Eero Ristolainen, Tampere University of Technology

Flip Chip Market Trends

A Compatibility Evaluation of Lead-Based and Lead-Free Solder Alloys in Conjunction with Electroless Nickel/Immersion Gold Flip Chip UBM
Scott Popelar, Andrew Strandjord, Bob Nieten, IC Interconnect

Lead-Free Solder Bump Technologies for Flip-Chip Packaging Applications
Zabeed S. Karim, Advanced Interconnect Teconology Ltd.; Rob Scbetty, Shipley LLC

Study of Underfill Resin Properties for High Performance Flip-Chip BGA Package
Yuko Sawada, Kozo Harada, Hirofumi Fujioka, Mitsubishi Electric Corporation

Novel Alignment Technologies for Wafer Level Packaging

Flip Chip Joining of Thin Chips on Flexible PEN Substrates
Erja Jokinen, Eero Ristolainen, Tampere University of Technology

THA2
Modeling & CAD
Session Chairs: Luu Nguyen, National Semiconductor Corp.; R. Panneer Selvam, University of Arkansas
8 am - 11:20 am

This session will address novel ways of modeling self and mutual frequency impedances of multiconductor in lossy substrates, equivalent circuit simulations of decoupling capacitors, thermomechanical warpage of packages with response surface methodology, CAD software for flip chip redistribution, characterization data on low loss PCB materials, thermal models for MEMS structures, and ultra wide bandwidth power devices modeling.

Controlling Capacitor Parasitics for High Frequency Decoupling
George Korony, Andrew Ritter, Carlos Gonzalez-Titman, Joseph Hock, John Galvagni, Robert Heistant, II, AVX Corp.

CAD Design for Area Pad Transformation
Yungul Huang, Spen-Li Fu, I-5HOU University; Cbing-Mai Ko, ASE TEST, Inc.

Computer Modeling to Optimize the Heat Removal Capacity of the Micro-Jet Array
R. Panneer Selvam, Yangki Jung, Joseph Kbater, S. Ang, A. Elshabini, University of Arkansas

The HP 85192B EEFet3 GaAs FET Nonlinear Model used in the High Efficiency Microwave Power Amplifier (HEMPA)
William H. Sims III, NASA - Marshal Space Flight Center

Analytic Model for Self and Mutual Frequency-Dependent Impedances of Multiconductor Interconnects on Lossy Silicon Substrates
Hasan Ymeri, Bart Nauwelaers, Katholieke Universiteit Leuven; Karen Maex, David De Roest, Michele Stucchi, IMEC

Electrical Evaluation of Differential Striplines for High-Speed Backplane using TDR/TDT Measurements
Youngmin Lee, Lucent Technologies; Keith Guinn, Kavita Goverdhanam, Agere Systems

THA3
Photonics
Session Chairs: Michael Wernle, NanoPierce Technologies; Phillip Zulaeta, Jet Propulsion Laboratory NASA
8 am - 11:20 am

The struggle for an economic solution to greater bandwidth, lower power, lower carrier loss and lower noise over long distances has propelled Photonics and Optoelectronics to the forefront of the telecommunications industry. However, the electronics packaging of photonic/optoelectronic devices has not occurred easily for larger volume applications. This session focuses on the design, material, fabrication and assembly issues associated with photonics/optoelectronics packaging and will also highlight selected applications of this rapidly growing technology.

A New Methodology for Comprehensive MEMS Packaging for Opto-Electronic Applications
R. Keusseyan, B. Speck, T. Mobley, DuPont Technologies

Optical Leak Testing of Hermetic Packages
John W. Newman, NorCom Systems Inc.

Angular Misalignments in Coupling a Wedged Single Mode Fiber to a Highly Elliptical Laser Diode
Z. Tang, R. Zbang, S. K. Mondal, F. G. Shi, J. Guo, University of California, Irvine

Electrical and Thermal Performance of a New Process for High Density LED Array Assembly
Michael E. Wernle, Michael Kober, NanoPierce Card Technologies GmbH

Stud Bump Flip Chip Assembly of MEMS and MOEMS
George A. Riley, FlipChips Dot Com

Assembly Considerations & Critical Processes for Optoelectronic Device Assembly
Bruce W. Huener, Palomar Technologies

THA4
Advanced Thick Film Materials Technologies
Session Chairs: Harry Kelzi, Teledyne Electronic Technologies; Mike Ehlert, National Semiconductor LTCC Foundry
8 am - 11:20 am

This round up of current topics features several papers on emerging methods of fine line patterning on ceramic and organic substrates and several other current issues. These include new paste systems for high thermal conductivity Aluminum Nitride substrates, an analysis of failure mechanisms in conductors on ceramic and a method of creating low impedance thin film decoupling caps for high-speed digital circuits.

A New Paste System for AlN
Christel Kretzschmar, Peter Otschik, Horst GrieBmann, Fraunhofer Institute for Ceramic Technologies and Sintering Materials
Thick Film Fine Line Patterning - A Definitive Discussion of the Alternatives
Meg Tredinnick, Peter Barnwell, David Malanga, Heraeus Inc., Circuit Materials Division

Direct Gravure Printing (DGP) Method for Printing Fine Line Electrical Circuits
Juha Hagberg, Marko Pudas, Marko Kittila, Seppo Leppavuori, University of Oulu

The Dependence of TFT Chemical Sensors on the Technology of Preparation Methods of Testing
Martin Adamek, Ivan Szendiuch, Technical University of Brno; Jan Krejci, Krejci Engineering

Fine Line Technology for BGA-Applications on Silicone Polymer Substrates
Gernot Bischoff, Gert Winkler, Technical Univ. of Ilmenau; Hubert Landeck KEW Konzeptentwicklung GmbH

The Mechanism and Prevention of Conductor Fracture on Printed Multilayer Ceramic and Low Temperature Co-fired Ceramic (LTCC) Substrates
Jiming Zhou, Stephen Tsai, Jerry Badgett, Christine Coapman, Delphi Delco Electronics Systems

Low Impedance Thin Film Decoupling Capacitor for High Speed Digital Circuits
S. Konushi, S. Nagakari, J. Takafuji, F. Fukumaru, S. Nambu, Kyocera Corporation

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