Flip Chip Technology & the End Market

William T. Chen
ASE

June 21 2004
A Quotation

“If a man can make a better mouse-trap, though he build his house in the woods, the world will make a beaten path to his door”

Att. Ralph Waldo Emerson
(1803 – 1882)
Brief History of Flip Chip

C4 on Ceramic Substrate in IBM 360 1965
   Evaporation 95/5 PbSn Process
Solder Bump Printing by Delco 1973
   Eutectic Solder
Invention of SLC on PWB in IBM 1986

Underfill Process developed in IBM 1987

High Volume Flip Chip BGA SRAM 1996
   Package shipped IBM
Industry Forecast – 1990s

In the mid 1990’s Industry forecasts have identified Flip Chip CSP/BGA as the package of the future.

The “Future” is here today. More device applications are designed into Flip Chip.

What are the industry factors that contribute to wide implementation of Flip Chip today?
Outline

- Semiconductor & Industry Trend
- Flip Chip Infrastructures
- Applications & the End Market
- Wrap-Up
Semiconductor & Industry Trends
World Semiconductor Forecast

Source: Gartner Dataquest June 2004
IC Capacity Growth & Feature Size Reduction

Source: Dataquest November 2003

WW Wafer production MSI/Qt

65nm
90nm
130nm
0.18 μm
0.25 μm
0.35μm
> = 0.5μm
Backend Growth: IDM & Subcon

Total Back-end 03-06 CAGR = 11.5%

Subcon 03-06 CAGR = 21.5%

IDM 03-06 CAGR = 5.4%

Subcon Backend Share Growth from 35% to 45%

Source: Dataquest
Paradigm shift in customer requirement to Integrated Solution

**Cost Focus**
- Economic scale to reduce cost and available capacity to meet overflow demand critical
- Leadframe-based packages
- Primarily packaging only

**Technology Focus**
- Advanced packaging and testing capabilities displace capacity as primary consideration, although cost remains important
- Substrate-based packages
- Packaging and increasingly testing

**Solution Focus**
- Integrated solution including substrate design and close partnership with complementary service providers to reduce cycle time becomes necessary, together with cost reduction and advanced technology
- Flip chip packages
- SiP, 3D Packaging
- Packaging, testing and materials required
Technology Evolution Changes The Value Chain

<table>
<thead>
<tr>
<th></th>
<th>PDIP</th>
<th>SOJ</th>
<th>QFP</th>
<th>BGA</th>
<th>Flip Chip</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leads</td>
<td>8</td>
<td>32</td>
<td>208</td>
<td>256</td>
<td>1100</td>
</tr>
</tbody>
</table>

**Technology Evolution**

- **Leadframe/Substrate**: LF/S
- **Inspect & Test**: Inspect/Test
- **Mold/Underfill**: Mold/UF
- **Wirebond/Bump**: WB/Bump
- **Other**

Source: Company estimates
Regional Shares of Semiconductor Consumption

Source: SIA June 2004
Industry Trends Summary

• Growth in volume and % of 130 nm & 90 nm devices.
• Increasing demand on SAT service providers for solutions
• Value chain evolution in cost to substrate.
• Semiconductor consumption growth shift to Asia Pacific.
Flip Chip Infrastructure
Flip Chip Implementation

Bumping, Wafer Probe, Assembly, Substrate, & Final Test Services

- Foundry
- Engineering Test Dev
- Substrate Design
- Substrate/Lead Frame Mfg
- Wafer Bumping/Probing
- Assembly
- Final Test

WLCSP, Module, System Assembly & Test

IC Circuit Design
Wafer Bumping

**BUMPING**

**WAFER SORT**

**SUBSTRATE**

**ASSEMBLY**

**FINAL TEST**

Substantial Capex Equipment & resource investment
Traditional part of major IDM’s wafer backend
Growing capabilities & capacities in Asia Pacific SAT’s
Broadening Bumping Offerings
  - Eutectic, high lead & lead free solders
  - Au for LCD applications
  - 150mm/200 mm/300 mm wafers from diverse foundries
Challenges in Cu-Low k & Pb free, electromigration
Growing application & market for WLCSP
Wafer Probing after Wafer Bumping
300/200/150 mm probing essential backend service
Few players with large probing & tester resources
Important not to be production/volume bottle neck
Challenges:
  - Test frequency
  - mixed signal/SIP/SOC
  - Bump pitch 150 um (array) & max bump counts
Key enabling Infrastructure with WLCSP
Build Up (BU) Substrate de facto standard for Flip Chip
Trend of Laser Via to replace Photoimagible Mat & Process
Substrate is major cost item in total package cost
BU substrate suppliers emerging outside Japan
Main users are microprocessor based companies
Design & assembly critical to package performance & cycle time
Laminate Substrate for low cost Flip Chip & FC CSP
Where “Rubber meets the Road” in FC Volume Manufacturing
Diverse BOM & Process to tackle Diverse Device, Bumps & Substrates
IDM inhouse s & SAT service suppliers Asia Pacific, US, Japan & Europe
Challenges in
  large dies, 90 nm Cu-low k devices,
  Green Package
  SIP & stacked dies & low cost CSP
electromigration
Final Test

- Major Capex & Resource Investments: user/customers have unique requirements
- Internal to IDM & few major SAT Service Suppliers
- Increasing volume requires more testers
- Significant maintenance costs
- Test Sockets, Handlers, Burn-in tools design & maintenances
- Technical Challenges
  - High frequency & power
  - RF, Mixed signal, SIP & SOC
  - Increase package size & ball count
Infrastructure

Essential Volume Manufacturing Capabilities for Turning Wafers into finished Flip Chip Packed devices.

Capabilities traditionally inside IDM’s
Growing Investments in Capabilities and Capacities in SAT Services suppliers

Enabling Flip Chip Implementations for all companies
High I/O & often with large dies
Share Bumping/Wafer Probe Capabilities with WLCSP
FA Infrastructure

Material Lab
- TMA
- DSC
- DMA
- FT-IR
- GC-MS
- AFM
- Auger ESCA...

Thermal Lab
- Ansys
- Flotherm
- Psksii- T
- Wind Tunnel
- VXI System...

Stress Lab
- I-DEAS
- ANSYS
- LS-DYNA
- AutoCAD
- Moire Interferometer
- Shadow Moire
- Electromigration...

Electrical/System Lab
- Electromigration
- Ansoft Spice Link
- HFSS/Quad
- Hspice
- Autocad
- 40 GHz Network Analyzer
- 50 GHz Probe
- EMC/EMI...

6"/8" / 12" Bumping
WLCSP
Fine-Pitch Wire Bonding
6"/8"/12” Flip Chip Assembly
SiP/Stacked-die
Green Technology

University & R&D Collaborations
- ITRI
- NCU
- NTU
- HKUST
- IMRE

FA Lab
- X-ray
- SAT
- TDR
- EDX
- AES/XPS
- SIMS...

Thermal Lab
Concurrent Engineering within Infrastructure

Fast Track Product Development

Customer → Tape Out

Wafer Fab → Wafer Out

ASE Bumping → Bump Mask Design → Bumping/Probing

ASE Assy → Package Design → Customer Approval → Tooling/Kit Preparation

ASE MTL → Review → Substrate Fabrication

ASE TEST → Program Engineering → Probe Card, Load & Burn-in Board Mfg. → Package Assembly → F/T
Four Generic Flip Chip Package Types

- **SiP Flip Chip**: RF Module, Networking, Graphics
- **HFC-BGA**: Graphics Chipset, Network Switching, Programmable Logic Device, Transmission, Workstation
- **FC-BGA**: Chipset, Graphics, CPU
- **FC-CSP**: RF Device, Power Regulator, Memory

Performance vs. I/O Count
Multi-Chip Flip Chip Examples
HFC BGA Family

Computer:   PC Graphics/Chipsets, Servers and High-End applications, Microprocessors for PCs & Servers, PDA, PLD.

Telecom:   Networking, Switching, Transmission, Cellular Base Stations.
FC BGA Family

Computer: PC Graphics/Chipsets, Server and High-End applications, Microprocessors for Servers, PLD, PDA.

Telecom: Network products (LAN), Switching, Transmission, Cellular base stations.
Flip Chip CSP Family

Consumer: Camcorders, Digital Cameras, PDA, DVD...

Computer: Voltage Regulators, High-Speed Memory, PC Cards, Peripherals...

Telecom: Pagers, Cellular Handsets,...
Device Applications & the End Markets
FC-CSP BY APPLICATION
Source: Prismark April 2004

**2002**
- Analog/Power Management: 2M, 20%
- ASIC/LOGIC: 4M, 40%
- DSP: 4M, 40%

Total: 10M Units

**2003**
- Analog/Power Management: 5M, 30%
- ASIC/LOGIC: 6M, 35%
- DSP: 6M, 35%

Total: 17M Units

**2007**
- Memory: 100M, 17%
- MCU/MPU: 100M, 17%
- ASIC/LOGIC: 15M, 3%
- Analog/Power Management: 75M, 13%
- DSP: 290M, 50%

Total: 580M Units
FLIP CHIP – PBGA CONSUMPTION BY DEVICE TYPE

2002
- MPU/MCU 10M 8.3%
- ASIC/Logic 17M 14%
- Chipset/MPR 73M 61%
- Graphics 3M 2.5%
- DSP 6M 5%

Total: 120M Units

2003
- MPU/MCU 16M 9%
- ASIC/Logic 25M 14%
- Chipset/MPR 95M 54%
- Graphics 17M 9.4%
- DSP 13M 7%

Total: 180M Units

2007
- MPU/MCU 50M 7%
- ASIC/Logic 101M 15%
- Chipset/MPR 288M 42%
- Graphics 137M 20%
- Memory 30M 4%
- DSP 76M 11%

Total: 682M Units

Source: Prismark April 2004
Semiconductor revenue forecast 2004 $199B
Source SIA June 2004
Three Flip Chip Applications End Markets

PC & Notebooks
- Microprocessors already in Flip Chip
- Increasing FC in Chipsets & Graphics Processors

Video Games
- Game Processors with heavy computing demand

Cell Phones
- FC CSP applications
- WLCSP
Wrap UP
Flip Chip is now Available to All

- Flip Chip implementation requires full infrastructure
- Flip Chip infrastructure growth in SATs
- Major end market in PC & Notebook expanding from Microprocessors to Chipsets & Graphic processor
- Projected expansion to Video Game ASIC Processors & Cell Phone Device Applications
- Major package solution for 90 nm devices & beyond
- WLCSP leveraging FC high volume production facilities for expanding applications and infrastructure growth
Thank you for your participation
Copyright © 2004 by Advanced Semiconductor Engineering, Inc.

All rights reserved.

Other company, product, or service names may be trademarks or service marks of others.

The materials in this presentation may not be reproduced, in whole or in part, in any manner or in any form or otherwise without the written permission of Advanced Semiconductor Engineering, Inc.