technical program

Tuesday, October 9
Plenary Program and Awards Ceremony
8 am - 9:40 am

Continental Breakfast at 7:45 AM

Refreshments in the Exhibit Hall: 9:40 am - 10:00 am

TA1

MEMS in Aerospace and Aeronautics Applications

Session Chair: John Champion, JHU Applied Physics Lab

10:10 am - 11:50 am

The utilization of MEMS enables a reduction of mass, volume, and electrical power, offering the opportunity for numerous solutions in space applications. The requirements for reductions in mass and volume are currently seen in the movements toward nano and pico satellites. Examples of how MEMS help in accomplishing these goals are given in the session papers.

Overview on current MEMS Fabrication Techniques and Applications
Michael Gaitan, NIST

MEMS in Aerospace Applications
Robert Osiander, The Johns Hopkins University/APL

MEMS in Space Science
Rainer K. Fettig, NASA Goddard Space Flight Center/ Raytheon ITSS

Micro-Scale Avionics Thermal Management
Matthew E. Moran, NASA GSFC

TA2

Next Generation Manufacturing Technology

Session Chairs: Nicole L Cavanah, Rockwell; Terry Baum, CTS RF Integrated Modules

10:10 am - 11:25 am

This session encompasses new developments in materials and processes. Developments in materials and processes are constantly pursued to meet customer requirements of cost, reliability, and size. The papers in this session will highlight new developments in wirebonding, LTCC, and advanced materials

A New Approach to Robust Wirebonding
Kenneth J. Huth, Semiconductor Packaging Materials

Ribbon Bondability Study of Chromium-Gold and Tantalum-Tantalum Nitride-Palladium-Gold Metallization
Jianbiao Pan, Robert M. Pafchek, Frank F. Judd, Jason Baxter, Lucent Technologies

Evaluation of Advanced Materials to Satisfy Higher Reflow and Solder Joint Life Requirements on MAP BGA
Trent A. Thompson, Motorola Semiconductor Products Sector

TA3

Microfabrication

Session Chair: Jay Jayaraj, Foster-Miller

10:10 am - 11:25 am

Increases in packaging density come from and through advances in density of all types of interconnections. This session illustrates several areas in which interconnect density enable performance or application improvements.

Fabrication and Assembly of Digital Transducer-to-Bus Interface Module (TBIM) with Directly Attached MEMS Device
Namsoo P. Kim, Nelli Amirgulyan, Chung-Ping Chien, Minas H. Tanielian, Boeing Co.

Development of Organic-Micromachined Interconnects on Si Substrates at Microwave Frequencies
D. Newlin, J. Harriss, A. Pham, J. P. Lee, Clemson University

Large Suspended Bondwire High Q Solenoid-type Inductors and SrTiO3 Thin Film Capacitors for Wireless Applications
Jae Y. Park, Yun S. Eo, Kye I. Jeon, Jong U. Bu, LG Electronics Institute of Technology

TA4

HD Organic Board Technologies

Session Chair: R. Wayne Johnson, Auburn University

10:10 am - 11:50 am

Vias are a critical issue in high density laminate substrate technology. Microvias and blind vias are two approaches to achieving higher routing densities. For laminate substrates used in packages, the solder mask is an integral layer between the laminate and the molding compound. Solder mask strength and crack resistance is important for package reliability. For flip chip assembly in the package, either the die is bumped or as described in the last paper, the bump can be fabricated as part of the PWB.

Moving to Microvias in a High Reliability, Low Production Environment
John Folkerts, Anne Dietrich, Paul Falk, Binh Le, Sharon Ling, Johns Hopkins University/ APL

Accuracy Enhancement of Blind via Depth-Controlled Drilling
Christian P. Williams, Johns Hopkins University

Strength Evaluation of Microelectronics Packaging Solder Mask Materials
Maurice Othieno, Thavarajah Manickam, Patrick Variot, Ramaswamy Ranganathan, LSI Logic Corporation

High Density Wiring Substrate with Molded Polymer-Core Bumps for Flip Chip CSP
Midori Kobayashi, Yasukazu Kishimoto, Toshiba Chemical Corporation; Kazuhito Higuchi, Susumu Kimijima, Toshiba Corporation

Student Reception

Tuesday, October 9, 2001
5:30 pm - 6:30 pm

sponsored by:

DuPont Microcircuit Materials
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TP1

Recent Development in Wafer Level Chip Scale Packages

Session Chairs: Beth Keser, Motorola Inc.; Michael Toepper, Fraunhofer IZM

2 pm - 5:25 pm

Wafer level CSP technologies are the fastest growing class of packaging technology currently in development. This rapid proliferation is being fueled by the need for package size minimization in a host of portable computing and communication products. This session addresses advancements that are being made in WLCSP process technologies which are aimed at cost effective minimal packaging with improved board level reliability.

A Polymer Reinforced WLP / Why It Has Superior Solder Joint Reliability
Deok-Hoon Kim, Peter Elenius, Scott Barrett, Flip Chip Technologies

Assembly and Reliability of a Wafer Scale CSP
Anthony Primavera, Universal Instruments; Parvez Patel, Motorola; K. Srihari, Binghamton University

Wafer Level CSP using a Screen Printing Technique
Hirokazu Ezawa, Masahiro Miyata, Masaharu Seto, Hiroshi Tazawa, Toshiba Corporation Semiconductor Company

On-Wafer Process for Stress-Free Area Array Floating Pads
Raymond A. Fillion, Robert J. Wojnarowski, Herbert Cole, Glenn Claydon, GE Corporate R&D

Indium Bump Bonding for Cryogenic Applications
Allen C. Keeney, David M. Lee, S. John Lehtonen, A. Shaun Francomacaro, Johns Hopkins University/APL

Low Cost Solder Bumping via Paste Reflow for Area Array Packages
Ning-Cheng Lee, Benlih Huang, Indium Corporation of America

A High Density Compliant Packaging Technology Development
Delin Li, Dave Light, Tessera Inc.

TP2

Wideband Materials Characterization for RF, Microwaves, and Wireless

Session Chairs: Michael Stein, Electro-Science Labs, Inc.; Peter Barnwell, Heraeus Circuit Materials Division

2 pm - 5:25 pm

The session deals with materials issues for both radio and microwave frequencies of the spectrum, with emphasis on lead-free, low-loss dielectrics, and photo patterned conductors compatible with low temperature cofired ceramic systems. RF & Microwave design and packaging engineers need vitally the acquisition of essential electrical high frequency data on various advanced electronic materials properties to serve various basic functions including interconnects. These materials data and information mainly include the complex dielectric constant, the material conductivity, and the attenuation component. The challenging design mandates additionally electronic products possessing specific desired electrical attributes, while still meeting basic thermal and mechanical essential requirements with high reliability and good yield.

High K Low Loss Dielectric Co-fireable with LTCC
Weiming Zhang, Matthias Scheikowski, Tom Hochheimer, Peter Barnwell, Heraeus Incorporated-Circuit Materials Division; Steve Dai, Motorola Labs.

Lead Free Dielectric Tape System for High Frequency Applications
Alvin Feingold, R. L. Wahlers, S. J. Stein, Electro-Science Labs, Inc.

RF Characterisation of No-Clean Solder Flux Residues
Maeve Duffy, PEI Technologies; Liam Floyd, Paul McCloskey, Sean Cian Ó Mathúna, NMRC; Karen Tellefsen, Mike Liberatore, A. Sreeram, Alpha Metals

Thick and Thin Film, High Density Packaging, Microwave, Integrated Passives
Michael R. Ehlert, Shaul Branchevsky, National Semiconductor LTCC Foundry

Photo Patterned Conductors with LTCC for Microwave and High Density Interconnect
Peter G. Barnwell, Brent Smith, Heraeus Circuit Materials Division; Michael Ehlert, National Semiconductor Corporation

High K, High Q LTCC Dielectric Material for Microwave Application
Yun-Hwi Park, J. H. Sung, D. H. Hwang, J. M. Lee, Y. K. Chung, Samsung Electro-Mechanics Co., Ltd.

High Permittivity Materials Development for LTCC
Michael T. Lanagan, Dean Anderson, Tom Shrout, Juan Nino, Hyuk-Joon Youn, Steve Perini, Clive Randall, Penn State University

TP3

Materials

Session Chairs: Herb Neuhaus, NanoPierce Technologies; Susan Bagen, Advanced Process Concepts

2 pm - 5:25 pm

Advances in materials are the key to microelectronics packaging. The papers in this session describe a number of advances in materials used in interconnect technology, and cover both board and assembly levels.

Z-axis Interconnection for 3-D High-Density Packaging
Silke Spiesshoefer, Leonard Schaper, Kaoru Maner, Errol Porter, Fred Barlow, George Bates, Mike Lucas, Bill Marsh, University of Arkansas; Michael Glover, Northrop Grumman

A Study on the Synthesis and Characterization of $AgInO_2$ Delafossite
Jane E. Clayton, Alan P. Constant, David P. Cann, Iowa State University

Characterization of $AlMgB_{14}$ Materials: An Ultra-hard Material
Theron Lewis, Alan Russell, Bruce Cook, Joel Harringa, Iowa State University

Pre-applied Flip Chip Attachment
Scott B. Charles, Michael Kropp, Robert Kinney, Steve Hackett, Robert Zenner, Bruce Li, 3M

Technology and Material for the CSP Flux-Free Underfill Resin and Process for Electrical Connection and Physical Adhesion at the Reflow Process Simultaneously
Kenji Kitamura, Naoki Kanagawa, Tomoaki Nemoto, Shoichi Fujimori, Shinji Hashimoto, Matsusita Electric Works, Ltd.

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Characterization of Ruthenia-Based Resistors Embedded in Low Temperature Co-fired Ceramic Substrates
Shen-Li Fu, Chi-Shiung His, I-Shou University

Screen-Printed Pb(Zr, Ti)$_{03}$ Thick Films for Ultrasonic Medical Imaging Applications
Marija Kosec, Janez Holc, Josef Stefan Institute; Franck Levassort, Louis Pascal Tran-Huu-Hue, Marc Lethiecq, LUSSI/GIP Ultrasons

TP4

Thermal Management

Session Chairs: Ajay P. Malshe, University of Arkansas; Tarak Railkar, Conexant

2 pm - 5:25 pm

Demands and advances in the thermal management area are highlighted in this session through various presentations by leading researchers on topics such as miniaturized heat pipes, reliability of high power optical devices, analysis and modeling.

Synthetic Jet Based Impingement Cooling Module for Electronic Cooling
Raghav Mahaligam, Nicolas Rumigny, Ari Glezer, Georgia Institute of Technology

Experimental Study of Miniature Heat Pipe with Composite Wick of Sintered/Woven Wire
Seok Hwan Moon, Ho Gyeong Yun, Gunn Hwang, Tae Goo Choy, ETRI

Thermal Control based on Miniature Heat Pipes for 3D MCM Packaging
Frederic Michard, M. Huan, C. Combes, D. Rousset, Alcatel Space Industries

Correlation of 980 nm Heat Pump Thermal Performance with Acoustic Microscopy (SAM) Results
Gabriel Takyi, C.Beesley, R.Baettig, A. Kendall, JDS Uniphase

Failure Mechanisms in High Power Optical Device Packaging: Semiconductor Laser Diodes - A Case Study
Ajay P. Malshe, Ajit R. Dhamdhere, S.N. Yedave, W.F. Schmidt, W.D. Brown, University of Arkansas (HiDEC-MEEG); John Morales, Coherent Semiconductor Group

Numerical and Experimental Simulation of Electro-Thermal Behavior of VLSI Chips
Z. J. Delalic, Jim Chen, Richard Cohen, Dennis Silage, Temple University

Set-Top Box Thermal Design with Detailed Modeling of High Power TBGA Packages
Sam Z. Zhao, Broadcom Corporation

TP5

High Density Packaging

Session Chairs: Rajen Chanchani, Sandia National Laboratories; Scott Popelar, IC Interconnect

2 pm - 5:25 pm

In this session, several advanced, high density substrate and MCM technologies will be presented. The first two papers report a new way to process organic laminate substrate and the photoimageable low temperature co-fired ceramic substrates, with fine features. A new 3D packaging technology with embedded active and passive devices will also be presented. Next, several papers also report MCM-D technology with variety of base substrate materials.

Total Pile Curing Substrate
Katsura Hayashi, Teruya Fujisaki, Masaaki Hori, Kyocera Co.

Novel Ceramic Packages and Architectures for MST Applications Made Possible with Photoimageable LTCC
Barry E. Taylor, Larry Bidwell, Angela Lawrence, DuPont i Technologies

High-Density Multi-Layer Thin-Film Packaging Technology for High-Performance ASIC Chips
Katsumi Kikuchi, Tadanori Shimoto, Hirokazu Honda, Keiichiro Kata, Koji Matsui, Sueo Morishige, NEC Corporation

A New 3-D Module using Embedded Actives and Passives
Yasuhiro Sugaya, Toshiyuki Asahi, Shingo Komatsu, Seiichi Nakatani, Matsushita Electric Industrial Co., Ltd.

A Multi-Layer Thin-Film MCM-D Modulator for VSAT Applications
Geert Carchon, P. Van Loock, K. Vaesen, S. Brebels, W. De Raedt, B. Nauwelaers, E. Beyne, IMEC-MCP/HDIP

The PSGA, A Lead-Free CSP for High Performance & High Reliable Packaging
Bart Vandevelde, Eric Beyne, Arun Chandreshekar, Evelien Driessens, Marcel Heerman, Jef Van Puymbroeck, IMEC

The Challenge of Overcoming Wire Sweep in Ultra-Fine-Pitch Wirebonded Ball Grid Array Packages
Robert Radke, Fuaida Harun, Ruzaini Ibrahim, Lois Yong, Tu-Anh Tran, Motorola Semiconductor Products Sector

Special Session*
2:00 PM – 3:20 PM

TP6

National Science Foundation and IMAPS Educational Foundation

Session Chair: Rao Tummala, Georgia Institute of Technology

Microwave Characterization of Low Temperature Cofire Ceramics with Embedded Fluid Channels
Orfirio Sanchez, Florida International University

Electrically Conductive Adhesives Technology
James E. Morris, TJ Watson School of Engineering & Applied Science

Efficient and Economical Laser Processing of Mixed Signal Packaging
T. Darren Brown, University of Kentucky

Mechanisms of the Adhesion of Aromatic Thermosetting Copolyesters (ATSPs)/SiO_2 and ATSPs/Polyimides
Amir Alam, University of Illinois at Urbana –Champaign

*Authors are NSF/IMAPS 2000 - 2001 Award Recipients

**Presentations will be 20 minutes each.*

IMAPS Annual Business Meeting

Tuesday, October 9, 2001
11:30 AM – Noon
Baltimore Convention Center

Change of Officers

Presidents' Messages to the Membership

Annual Business Meeting

No lunch will be provided at this meeting

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WA1

High Density Packaging for Portable Terminal Equipment in Japan *(Japanese Translated Session)*

Session Chairs: Yuzo Shimada, NEC Corporation; Charles E. Bauer, TechLead Corporation

8 am - 10:55 am

The leaders in mobile electronics product and technology for more than 40 years, Japan now leads again in the application of flip chip packaging techniques for today's portable consumer products. This session presents current deployment alternatives for flip chip in Japanese products and demonstrates cost effective flip chip use in telecommunication appliances, personal computing devices and other mobile products.

High Density Packaging Using Flip Chip Technology in Mobile Communication Equipment
Kazuto Nishida, Matsushita Electric Industrial Co., Ltd.

Assembly Technology for Miniaturizing of Advanced Cellular Phone
Tadao Otani, Toshiba Corporation

LTCC Module Using Flip Chip Technology for Mobile Apparatus
Jitsuho Hirota, Murata Manufacturing Co., Ltd.

The Technology of Flip Chip Bonding on Organic Substrate for PDA
Akira Makabe, Seiko Epson Corporation

Packaging Technology for Mobile PCs
Shunichi Kikuchi, Fujitsu Limited

Sn-Zn Lead-free Solder Applied Notebook Personal Computer
Motoji Suzuki, NEC Corporation

WA2

Integrated Passives in LTCC for RF, Microwaves and Wireless

Session Chairs: John Gipprich, Northrop-Grumman; Fred Barlow, University of Arkansas

8 am - 11:20 am

The session deals with integrated passives in low temperature cofired ceramic systems. Thermal management is a crucial issue to be addressed in the LTCC manufacturing process, as a potential emerging technology for telecommunications, including instrumentation, military, space, satellite communications, adaptive antennas, data and wireless transmission, directions finder, radar, electronic counter measures, threshold detection, local area networks, cellular & personal communications services (PCS), GPS, ISM, and wireless market driven products in general. Components and break through trends in passives integration, advanced devices, and elaborate systems evolve as the drive mandates higher circuit densities and realization of finer pitch patterns (reducing device junction temperature and improving the thermal resistance of the various interfaces of the planar electronic materials).

Parameterized Libraries of Embedded Inductors and Capacitors in LTCC
R. Ramprasad, Feng Ling, William Blood, Thomas Myers, Michael Petras, Aykut Dengi, Mel Miller, Motorola, Inc.

A Packaged Miniature Antenna for Wireless Networking
Bedri A. Cetiner, Luis Jofre, Franco de Flaviis, University of California

Efficient Band Pass Filter Design for a 25 GHz LTCC Multichip Module using Hybrid Optimization
Winfried Simon, Reinhard Kulke, Andreas Lauer, Matthias Rittweger, Peter Waldow, Ingo Wolff, IMST GmbH

Power Distribution Networks in Multilayer LTCC for Microwave Applications
Reinhard Kulke, Winfried Simon, Gregor Moellenbeck, Juergen Kassner, Peter Uhlig, Peter Waldow, IMST GmbH

Manufacturing of Multilayer Dielectric Ceramic Chip Antenna for Bluetooth by Using LTCC Technology
Hyun Hak Kim, Jong Yeon Lee, Tae Seok Park, Jong Myung Woo, Samsung Electro-Mechanics Company

Effect of Design and Processing Parameters on Buried Resistors in LTCC Systems
Aicha Elshabini, V. Rajagopalan, F. Barlow, W. Gangqiang, S. Ang, A. Elshabini, University of Arkansas

Glass-Ceramic Module for 60GHz-Band Wireless Communication Systems
Kazuhiro Ikuina, Takeya Hashiguchi, Masaharu Itoh, Kenichi Maruhashi, Keiichi Ohata, NEC Corporation

WA3

Advanced Wirebond

Session Chairs: Lee Levine, Agere Systems; William Greig, Greig Associates

8 am - 10:55 am

This session will expand our understanding of wire bonding process mechanisms. Although wire bonding is the most common form of IC interconnection, the welding mechanisms have not been fuly explained. The papers in this session describe DOEs using in situ sensors and advanced ultrasonic systems that expand our understanding of wire bonding and provide process capability improvements.

In-Situ Ultrasonic Stress Microsensor for Second Bond Characterization
Juergen Schwizer, Oliver Brand, Henry Baltes, ETH Zurich; Michael Mayer, ESEC Cham

Wire Bond Temperature Sensor
Shivesh K. Suman, Yogendra Joshi, University of Maryland; Michael Gaitan, George Harman, NIST

High Frequency Wirebonding: Its Impact on Bonding Machine Parameters and MCM Substrate Bondability
Harry K. Charles, Jr., S. John Lehtonen, Katherine J. Mach, Jean S. DeBoy, Richard L. Edwards, The Johns Hopkins University/APL

The Influence of Surface Defect Size on the Wire Bond Pull Strength for Automotive Lead Frame Materials
Philip W. Lees, David W. M. Williams, Barry Njoes, Eric Dextradeur, Technical Materials, Inc.

Fine Pitch 2nd Bond Evaluation for PBGA Packages: Process Capability and Reliability Assessments
Tu Anh Tran, Greg Ridsdale, Lois Yong, Burt Carpenter, Dennis Ravenscraft, Fuaida Harun, Motorola

Wire Loop Development for Advanced PBGA Packages with Multiple Rows of Bonding Fingers and Power-Ground Rings
William K. Shu, Philips Semiconductor

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technical program

WA4

Power Packaging

Session Chairs: Doug Hopkins, State University of New York; Dave Kellerman, Material Solutions® Corporation

8 am - 10:55 am

Higher power density packaging is being addressed on several technological levels. Materials and processes are being developed and applied in high power density packaging including Cubic Boron Nitride, a novel LTCC/silver metal structure, a new thermally conductive die attach material, and diamond/diamond like film materials. The papers present structures to promote power in RF, MCM and discrete MOSFETS.

High Thermal Conductivity Cubic Boron Nitride Thick Films
Peter J. Gielisse, Halina Niculescu, Jason P. Tremblay, Selim Achmatowicz, Malgorzata Jakubowska, Elzbieta Zwierkowska, Leszek J.Golonka, Tomasz Zawada, Viktor B. Shipilo, Elena Shishonok, Ludmila M. Gameza, Florida State University

Thick Silver Tape in Low Temperature Cofired Ceramic (LTCC) for Thermal Management
W. Kinzy Jones, Peng Wang, Yanqing Liu, Florida International University

Silicon Carbide Power Die Packaging in Diamond Substrate Multichip Power Module Applications
Alex Lostetter, K. J. Olejniczak, A. P. Malshe, W. D. Brown, Aicha Elshabini, University of Arkansas

Evaluation of Embedded Power Technology for IPEM Packaging Applications
Zhenxian Liang, Fred C. Lee, J. D. Van Wyk, G-Q. Lu, Virginia Tech

Hybrid Modules as an Alternative to Paralleled Discrete Devices
Don Morozowich, Robin Farruggia, Powerex, Inc.

High Efficiency Microwave Power Amplifier: From the Lab to Industry
William H. Sims, NASA - Marshal Space Flight Center

WP1

Reliability of Novel CSP Structures

Session Chairs: Ernie Vasvary, Micro Systems Engineering Inc.; James Cook, Promex

2 pm - 5:25 pm

CSP technologies are key drivers to the industry's continuing need for form factor reduction and/or improved functional integration. These technologies must also be able to withstand the stresses that hand held products are often subjected to. This session will address a range of topics related to mechanical modeling or reliability testing of CSPs at the component and board level.

Strength Characterization and Fracture Surface Analysis of Silicon Dies
Jenq-Dah Wu, S. H. Ho, Sarah Liao, P. J. Zheng, Henry Iksan, Advanced Semiconductor Engineering, Inc

Reliability Design and Experimental Work for Mirror Image CSP Assembly
Dongji Xie, Sammy Yi, Kazu Nakajima, Flextronics International

Reliability and Failure Mechanisms of Chip Scale Package on Laminate Technology
Zsolt Illyefalvi-Vitez, Pál Németh, Péter Bojta, Technical University of Budapest

FEM Analysis of Solder Pad Warpage in Elastomer Attaching Process
Jong-Kul Lee, Byoung Un Kang, Hyuk-Soo Moon, Tae-Sung Kim, LG Cable Ltd., Microelectronic Materials T/G

Reliability Evaluation of CSP Electronic Devices Package
Hideo Koguchi, Chie Sasaki, Kazuto Nishida, Nagaoka University of Technology

The Effect of Compound Properties to Three Dimension Packages
Caesar Lin, Y. P. Wang, T. D. Her, Siliconware Precision Industries Co., Ltd.

Design and Reliability Study of Wire-Bonded µBGA® Packages for DDR-DRAM Applications
Ilyas Mohammed, Sridhar Krishnan, Young-Gon Kim, Tessera, Inc.

WP2

Integrated Passive Technology with PWB & Thin Film Processing for RF and High Speed Applications

Session Chairs: Robert Heistand, AVX; Timothy Lenihan, Sheldahl

2 pm - 5:25 pm

Integrated passive technology is being driven by the RF/wireless and high speed signal integrity applications. This session focuses on technology being developed in the printed wiring board and thin film fabrication arenas. Common themes are the innovations to increase specific capacitance, or raise the Q of inductor elements available for integration. Papers are selected from academia, material suppliers and systems houses.

Thin Film Capacitors Embedded into High Density Printed Circuit Boards
Angus I. Kingon, J-P Maria, TY Kim, North Carolina State University; R. Crosswell, Motorola

Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards
William Borland, John J. Felten, DuPont Electronic Materials

Lead-free High K Dielectrics for Integral Capacitor using MOCVD
Tatsuo Ogawa, Ahmet Erbil, Swapan K. Bhattacharya, Georgia Institute of Technology

The Effect of Miniaturization of Embedded Resistors in High Density Substrates
Daniel Brandler, Ohmega Technologies, Inc.

The Integration of RF Passives using Thin Film Technology on High-Ohmic Si in Combination with Thick Film Interconnect
Joost Van Beek, Marc van Delden, Andre Jansman, Arjen Boogaard, Nick Pulsford, Arnold den Dekker, Philips Research

RF Integrated Passives in Three Dimensions
Theo G.S.M. Rijks, J.T.M. van Beek, A.B.M. Jansman, M.K. Kammerer, Philips Research

High-Value, Low-Loss MOS Capacitors for RF Decoupling
Fred Roozeboom, R. Elfrink, T. Rijks, J. Verhoeven, A. Kemmeren, J. van den Meerakker, Philips Research

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WP3

Cu Wirebond and Reliability

Session Chairs: Michael Sheaffer, K&S Packaging Materials Group; Roupen Keusseyan, Dupont

2 pm - 5:25 pm

Copper metallization (bond pads) and low K dielectrics represent the next challenge facing IC manufacturing. Advanced wire bonding techniques are required for interconnection. This session will address interconnection issues for copper metallized integrated circuits. Wire bond reliability in highly stressed and corrosive environments will also be addressed.

Wire Bonding to Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks and Materials Considerations
George G. Harman, Christian E. Johnson, NIST

Research on Prevention of Corrosion at Au-Al Bonds
Yasuhide Ohno, Takuo Shoji, Keishi Miyamoto, Isao Shimizu, Kumamoto University

Reliability of Aluminum Wirebonds in Plastic Encapsulated Packages
Pankaj Mithal, Delphi Delco Electronics

Wirebonds for Munitions Applications: Effects of Dynamic Shock, Vibration, and Spin
S. John Lehtonen, H. K. Charles, Jr., Johns Hopkins University/APL; G. Katulka, Peter Muller, N. Hundley, M. Ridgley, ARL

Back-end Assembly Solution to Bare Copper Bond Pad Wafers
Chuchung Lee, Susan Downey, Peter Harper, Bill Williams, Fuaida Harun, C. C. Yong, Motorola

A Reliable Copper Wire Bond Interface for Microelectronic Packaging
Nicole Cavanah, Rockwell International

Differences Between Aluminum and Copper Wafer Metallization in the Wafer Saw Process for Thin BGA Packages
Mark Gerber, Noel Arguello, Daniel Cavasin, Motorola-SPS

Lunch in the Exhibit Hall

Tuesday & Wednesday
October 9th & 10th
Noon - 2 PM

WP4

Lead-Free Solders

Session Chairs: R. Wayne Johnson, Auburn University; Herb Neuhaus, NanoPierce Technologies

2 pm - 5:25 pm

The electronics industry is moving to lead free assembly for environmental and market driven reasons. Solder alloys, fluxes, processing equipment, mechanical properties, and reliability are all issues that must be addressed prior to the switch to lead-free assembly. It is a very complex undertaking and this session will examine some of the key points.

Effects of Cu or Bi Additions to the Creep Properties of Sn-3.5Ag Solder Alloy Joints
S. W. Shin, D. K. Joo, Y. S. Lee, Jin Yu, Korea Advanced Institute of Science and Technology

Best Composition for Sn-Ag-Cu Lead-Free Solder
Katsuaki Suganuma, G. Kim, S. H. Huh, Osaka University

Solder Paste with Polymerizing Flux for Lead-Free Alloy Solder
Tsutomu Nishina, Kenji Okamoto, Fuji Electric Corporate Research and Development, Ltd.

Improvement of Wave Soldering Equipment for Lead-Free Solder
Shigeo Nomura, Makoto Miyazaki, Kenichi Oki, Toshiyasu Takei, Akio Yoshida, Shigeyuki Ogata, Oki Electronics Industry Co., Ltd.

Soldering Property of BGA using Sn-Bi System Solder Balls
Toshiya Akamatsu, Kazuyuki Imamura, Fujitsu Laboratories Ltd.

Thermal and Mechanical Cycling Fatigue of PBGA Assemblies with Lead-Free Solder Pastes
Krishna Jonnalagadda, Tao Bai, Bill Olson, Motorola Labs (ATC)

Ultra Low Alpha Emission Lead Free Solder for Flip Chip Bumps
Yasushi Moriwaka, Satoru Takahashi, Masayoshi Kohinata, Naoki Uchiyama, Mitsubishi Materials Corporation

Interactive Forum (Poster Session)

1 pm - 4 pm

Compact Folded-Line RF Power Dividers
Chi-Young Lim, R. S. Settaluri, V. K. Tripathi, A. Weisshaar, Oregon State University

85°C/85%RH or 40°C/95%RH? Contradictory Results in Climatic Reliability Tests
Gabor Harsanyi, Budapest University of Technology and Economics - Hungary

Alternative Underfill Material for CSP Packages: Low Outgassing and Ionics Epoxy
Michael Ko, 3M; Chin Teong Ong, 3M - Singapore

Modeling of Effects of Geometry and Temperature Cycle on Viscoplastic Deformation and Durability of FCOC Solder Joints
Qian Zhang, Yogendra Joshi, Abhijit Dasgupta, Rathindra Pal, University of Maryland

Zero Shrink Process for Cost Sensitive High Volume LTCC Applications
Mike F. Barker, Rick Draudt, DuPont Microcircuit Materials

Inexpensive Processes for Flip Chip Manufacturing
Karel Malysz, Ivan Szendiuch, Technical University of Brno - Czech Republic

Development of a Low Volume Flexible Flip Chip Process
Alan P. Boone, Rockwell International

A New Thermally Conductive Die Attach Film with Low Stress and Excellent Reliability as a Replacement for Lead Solders
Takashi Masuko, Hiroki Hayashi, Shinji Takeda, Junko Morikawa, Toshimasa Hashimoto, Hitachi Chemical Co., Ltd.

Reliability of Bumpless TAB Component: CSPs and Bare Dies, for Harsh Environment Applications
Daniel Lambert, Danielle Roze, Patrick Courant, Bull TPAM

A Study of the Effect of Fabrication Parameter Variation on Thick Film Strain Gauge Characteristics
Yulan Zheng, John Atkinson, Russ Sion, Gary Zhang, University of Southampton

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Poster Papers continued......

OptoBGA™ for 10Gbps Data Link
Masahiro Kijima, Mitsuo Yanagisawa, Kyocera Corporation

Radiation Tolerant Computer for Space Environment
Anthony S. Lai, Steve Motter, Brian Dietz, Aitech Space Systems Inc.

New Direct-Write Technology for Pad Redistribution on Individual Die
Michael T. Duignan, Scott A. Mathews, David N. Wells, Daniel Anthony, Potomac Photonics, Inc.

Power Cycling and Structural Integrity Approach to Assessing Reliability of Electronic Packaging
Bor Zen Hong, Tsorng-Dih Yuan, IBM Microelectronics Division

The New Microelectronic Ignition Circuits for Sodium and Metal Halide Lamps
Janusz J. Gondek, M. Ciez, J. Kocol, W. Zaraska, Private Institute of Electronic Engineering

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Denver, CO • September 4-6, 2002

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Technical Program Chair: **Rick Charbonneau**, StorageTek
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THA1
Flip Chip
Session Chairs: Andrew Strandjord, IC Interconnect; Philip Garrou, Dow Chemical
8 am - 11:20 am

This session will be led by a survey of new flip chip applications and markets. New flip chip bumping technologies, lead-free solder alternatives, very fine pitch solder bumps and indium solders will also be discussed in this session.

Flip Chip Market Trends
E. Jan Vardaman, Linda Matthew, TechSearch International, Inc.

Lead-Free Solder Alloys for Flip Chip Applications Using Stencil Printing
Scott Popelar, Andrew Strandjord, Larry Heitz, IC Interconnect

Lead-Free Solder Bump Technologies for Flip-Chip Packaging Applications
Zaheed S. Karim, Rob Schetty, Advanced Interconnect Techonology Ltd.

Low Cost Flip Chip on Paper Assembly Utilizing Non-Thermal Cure Materials
Jad Rasul, Jan Danvir, Noel Eberhardt, Ali Tootoonchi, Motorola Inc.

Study of Underfill Resin Properties for High Performance Flip-Chip BGA Package
Yuko Sawada, Kozo Harada, Hirofumi Fujioka, Mitsubishi Electric Corporation

Novel Alignment Technologies for Wafer Level Packaging
Friedrich P. Lindner, Christian Schaefer, Bob Michaels, Thomas Glinsner, EV Group

Flip Chip Joining of Thin Chips on Flexible PEN Substrates
Erja Jokinen, Eero Ristolainen, Tampere University of Technology

IMAPS 2001 PROCEEDINGS

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THA2
Modeling & CAD
Session Chairs: Luu Nguyen, National Semiconductor Corp.; R. Panneer Selvam, University of Arkansas
8 am - 11:20 am

This session will address novel ways of modeling self and mutual frequency impedances of multiconductors in lossy substrates, equivalent circuit simulations of decoupling capacitors, thermomechanical warpage of packages with response surface methodology, CAD software for flip chip redistribution, characterization data on low loss PCB materials, thermal models for MEMS structures, and ultrawide bandwidth power devices modeling.

Improved Thermomechanical Warpage Prediction of Microelectronic Packages Using Response Surface Methodology
Eric Egan, Gerard Kelly, Tom O'Donovan, Peter Kennedy, NMRC

Controlling Capacitor Parasitics for High Frequency Decoupling
Andrew Ritter, George Korony, Carlos Gonzalez-Titman, Joseph Hock, John Galvagni, Robert Heistant, II, AVX Corp.

CAD Design for Area Pad Transformation
Yu-Jung Huang, Ching-Mai Ko, Shen-Li Fu, I-SHOU University

Computer Modeling to Optimize the Heat Removal Capacity of the Micro-Jet Array
R. Panneer Selvam, Joseph Khater, Yangki Jung, S. Ang, A. Elshabini, University of Arkansas

The HP 85192B EEFet3 GaAs FET Nonlinear Model used in the High Efficiency Microwave Power Amplifier (HEMPA)
William H. Sims, NASA - Marshal Space Flight Center

Analytic Model for Self and Mutual Frequency-Dependent Impedances of Multiconductor Interconnects on Lossy Silicon Substrates
Hasan Ymeri, Bart Nauwelaers, Karen Maex, David De Roest, Michele Stucchi, Katholieke Universiteit Leuven

Electrical Evaluation of Differential Striplines for High-Speed Backplane using TRD/TDT Measurements
Youngmin Lee, Keith Guinn, Kavita Goverdhanam, Agere Systems

THA3
Photonics
Session Chairs: Michael Wernle, NanoPierce Technologies; Phillip Zulueta, Jet Propulsion Laboratory NASA
8 am - 11:20 am

The struggle for an economic solution to greater bandwidth, lower power, lower carrier loss and lower noise over long distances has propelled Photonics and Optoelectronics to the forefront of the telecommunications industry. However, the electronics packaging of photonic/optoelectronic devices has not occurred easily for larger volume applications. This session focuses on the design, material, fabrication and assembly issues associated with photonics/optoelectronics packaging and will also highlight selected applications of this rapidly growing technology.

Design for Reliability of MEMS / MOEMS for Lightwave Telecommunications
Susanne Arney, Lucent Technologies Bell Labs

A New Methodology for Comprehensive MEMS Packaging for Opto-Electronic Applications
Roupen L. Keusseyan, D. Amey, M. Doyle, S. Horowitz, J. Sosnowski, DuPont Microcircuit Materials

Angular Alignment Considerations in Laser Diode to Microlensed Optical Fiber for Automated Photonics Packaging
Zirong Tang, Frank G. Shi, University of California, Irvine

Electrical and Thermal Performance of a New Process for High Density LED Array Assembly
Michael E. Wernle, Michael Kober, NanoPierce Card Technologies GmbH

Assembly Considerations & Critical Processes for Optoelectronic Device Assembly
Bruce W. Hueners, Palomar Technologies, Inc.

Stud Bump Flip Chip Assembly of MEMS and MOEMS
George A. Riley, FlipChips Dot Com

Optical Leak Testing of Hermetic Packages
John W. Newman, NorCom Systems, Inc.

THA4
Advanced Thick Film Materials Technologies
Session Chairs: Harry Kellzi, Teledyne Electronic Technologies; Mike Ehlert, National Semiconductor LTCC Foundry
8 am - 11:20 am

This round up of current topics features several papers on emerging methods of fine line patterning on ceramic and organic substrates and several other current issues. These include new paste systems for high thermal conductivity Aluminum Nitride substrates, an analysis of failure mechanisms in conductors on ceramic and a method of creating low impedance thin film decoupling caps for high-speed digital circuits.

A New Paste System for AIN
Christel Kretzschmar, P. Otschik, H. GrieBmann, Fraunhofer Institute for Ceramic Technologies and Sintering Materials

Thick Film Fine Line Patterning - A Definitive Discussion of the Alternatives
Meg Tredinnick, David Malanga, Peter Barnwell, Heraeus Incorporated-Circuit Materials Division

Direct Gravure Printing (DGP) Method for Printing Fine Line Electrical Circuits
Juha Hagberg, Marko Pudas, Seppo Leppavuori, Microelectronics Laboratory and EMPART Research Group of Infotech Oulu

Sub-400C, Direct Write-able Dielectrics and Conductors for Polyimide and Other Low-T Substrates
Paul G. Clem, Nelson S. Bell, Geoff L. Brennecka, Duane B. Dimos, Sandia National Laboratiories

Fine Line Technology for BGA-Applications on Silicone Polymer Substrates
Gernot Bischoff, Gert Winkler, Technical Univ. of Ilmenau; Hubert Landeck KEW Konzeptentwicklung GmbH

The Mechanism of Thick Film Conductor Fracture on Printed Multilayer Ceramic and LTCC Substrates
Jiming Zhou, Stephen Tsai, Christine Coapman, Delphi Delco Electronics Systems

Low Impedance Thin Film Decoupling Capacitor for High Speed Digital Circuits
Shigeo Konushi, S. Nagakari, J. Takafuji, F. Fukumaru, S. Nambu, Kyocera Corporation

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Thanks!

Refreshment Breaks

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Tuesday: 9:40 am - 10:00 am
Wednesday - Thursday: 9:15 am - 9:40 am

Tuesday - Wednesday: 3:15 pm - 3:45 pm

All breaks will be in the Exhibit Hall

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