Advance Program and Registration

Microelectronics - the bridge to the future!

Hynes Convention Center
Boston, Massachusetts
November 16 - 20, 2003

EXHIBITION:
November 18 - 20, 2003

CONFERENCE & EVENTS:
November 16 - 20, 2003

FEATURING:
♦ 25 Technical Sessions
♦ Special Poster Session
♦ 14 Professional Development Courses

....and back by popular demand
“Hands-on” Factory Training Workshop

Program, Exhibition and Registration Information: www.imaps2003.org

Endorsed by the American Ceramic Society
On behalf of the IMAPS 2003 Symposium Committee (SymCom_2003) and the IMAPS New England Chapter, I invite all of you to attend the 36th International Symposium on Microelectronics and to visit the preeminent historic, cultural and dynamic city in the US that epitomizes the “The Spirit of America”.

This year’s symposium will be held at the Hynes Convention Center in Downtown Boston from 16-20th November 2003.

The Technical Subcommittee and The National Technical Committee have assembled an incredible program consisting of Professional Development Courses (PDC) offered on Sunday & Monday, 16th and 17th, November and Technical Sessions offered on Tuesday, Wednesday & Thursday, 18th-20th November. A half-day FREE PDC is also being offered to registered students only.

The Spouse/Guest program promises exciting forays to the picturesque North Shore, “historic Salem” and interesting Plymouth Plantation areas of Massachusetts.

The Student Subcommittee in addition to sponsoring several students’ related activities is also sponsoring a Student Marketing Competition and an Employment Center.

One can see from the above that your SymCom_2003 has completed all of the arrangements that will result in a successful symposium. However, without sufficient support from our Exhibitors, the Symposium would struggle to also be a commercial success - which is a necessity!

With this in view, we will be serving a buffet style luncheon in the exhibits hall to all participants and guests during the exhibit hours. This is per the wishes of our Exhibitors. Attendees please take advantage of this opportunity to visit the exhibits area and stop by as many booths as possible during your stay.

Additionally, we are working with exhibitors to present a “Manufacturers’ Demonstration Line” (Demo Line) in the Exhibit Hall and also The “Exhibitor State-of-the-Art Presentations” (ESAP), which will give exhibiting companies a 15-minute session to present, via PowerPoint presentation, whatever products and services they deem important for the assembled audience. These sessions will be held during exhibit hall hours on the exhibit floor.

The improving geopolitical situation and the excellent attendance at the recent NE Annual Symposium are two leading indicators that predict an improving economy. As General Chair I am beseeching all potential Exhibitors to “get with the spirit” and sign on for exhibit booths! Don’t get left behind!

The IMAPS 2003 Symposium Committee is working enthusiastically with the National Committee, the NE IMAPS Committee and the HQ staff to make this an exciting and worthwhile endeavor for all.

Come and see how “Revolutionary Things Happen in Boston!” - see you in November.

Delip “Doug” Bokil
Environmental Systems Products
doug.bokil@etest.com
Greetings from Boston and New England where the American Industrial Revolution began. Historic Boston is the right place for us to gather with leadership in so many fields of Emerging Technologies that include MEMS, advanced photonics and a variety of biomedical areas. Come and enjoy the region and its rich heritage, home to Ivy League Universities like Harvard and world-renowned technical institutes like MIT. New England is populated with hundreds of advanced technology companies, including the world’s most successful MEMS company and the first Nanotech materials manufacturer. IMAPS 2003 International Symposium will also celebrate triumphs of technology and the resurgence of a stronger tech-driven economy. Hear and meet local talent as well as world authorities who will be guests and speakers.

We have a strong suite of technical programming that includes excellent papers from around the world and timely Professional Development Course (PDC) topics. Once again, we will have our special event describing the very latest packaging and related technologies in the Japanese Translations Session. Learn the latest trends in well-established areas like ceramics, but also find out what’s happening in emerging technologies where convergence raises the bar for versatility and performance. The pent up, overdue demand for new high-tech products coupled with an array of ready-to-launch developments will bring energy and excitement. Boston is the #1 IMAPS venue and the 2003 Symposium will be a very significant advanced technology event.

We have 25 sessions that thoroughly cover all important topics in electronic materials, interconnects and packaging. Interconnect systems include advanced ceramic materials and designs such as LTCC and embedded passives. Organic circuitry topics include high-density structures, micro-fabrication processes and high-speed materials for the new telecom. Packaging is well represented with a number of sessions that encompass advanced thick film, very fine pitch, high density, power device packaging, thermal management and RF systems. The most advanced packaging trends are detailed; flex-based chip carriers, Flip Chip, CSPs, and wafer-level packaging (WLP) processes.

The PDCs are diversified with timely themes that cover economics, manufacturing, business strategy, and Emerging Technology including “printed organics,” Flip Chip and new underfills, innovative sensors, Nanotechnology, MEMS and MOEMS. We have not neglected the all-important established methods and will include printing, soldering, LTCC, plating, lead-free materials, wire bonding, product launch marketing, six-sigma quality, and many others.

IMAPS enthusiastically welcomes students and provides support through a strong scholarship program. There are several student events and sessions this year. Winners of the Student Marketing Campaign contest will be announced and there will be a tour to an advanced MEMS software and logistics company. The poster sessions and educational forums will give students a voice, a chance to discuss ideas, and a means to interact with peers and industry.

Come network and socialize with friends, colleagues and world experts who will all be there. Boston is America’s gateway to the oldest and the newest – to science and the arts, to the past and to the future. And the newly completed transportation network (including the famous “Big Dig”) is ready to help make this a memorable and rewarding journey. So don’t be left behind as the world gets back on track and technology leads the way to good times.

See you soon in Boston to help launch the Revolution.

Onward,

K Gilleo
ET-Trends LLC
gilleo@ieee.org

Welcome Reception
Monday, November 17
6:00 – 8:00 PM
at the
The Sheraton Boston Hotel

INTERESTED IN EXHIBITING? CONTACT IMAPS TODAY • 1-202-548-4001 OR E-MAIL DPAUL@IMAPS.ORG
SAVE UP TO $50 OFF FULL-SYMP pleasure REGISTRATION BY REGISTERING ON-LINE: WWW.IMAPS2003.ORG

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What Your 2003 Full Symposium Registration Includes

Your registration includes the Awards Ceremony, Technical Sessions, Marketing Forum, Exhibits, Welcome Reception, Exhibit Hall Lunch, 2003 Proceedings (printed & CD-ROM Versions), and an automatic one-year IMAPS membership renewal for individual and student members in good standing at the time of registration. For an additional fee you can register for the Professional Development Courses (PDC), Golf Tournament, and the Spouse/Guest Program.

IMAPS 2003 Registration Hours

Sunday Nov. 16 8:00 AM – 5:00 PM
Monday Nov. 17 8:00 AM – 5:00 PM
Tuesday Nov. 18 7:00 AM – 5:00 PM
Wednesday Nov. 19 7:00 AM – 5:00 PM
Thursday Nov. 20 7:00 AM – Noon

Exhibit Hours

Tuesday Nov. 18 9:00 AM – 5 PM
Wednesday Nov. 19 9:00 AM – 5 PM
Thursday Nov. 20 9:00 AM – Noon

As of July 30, 2003, email address will change to @comcast.com
The 9th Annual IMAPS Golf Classic will be held at Pinehills Golf Club – Plymouth on Monday, November 17, 2003. The tournament will feature a shotgun start with prizes awarded to the overall winners, as well as those closest to the pin and with the longest drive.

Pinehills Golf Club, Plymouth, MA. [www.pinehillsgolf.com](http://www.pinehillsgolf.com)

**Pinehills Golf Club** was created to rival the country’s most prestigious golf clubs, bringing world class, daily fee golf to New England. An unparalleled range of comprehensive facilities, attentive service and a commitment to excellence are the hallmarks of Pinehills, which is dedicated to offering players of all levels a “total golf” experience in keeping with the rich traditions of the world’s greatest game.

Over 300 acres of rolling hills punctuated by dramatic, glacially carved kettles and kames is the setting for two, new 18 hole championship courses designed by Rees Jones and Nicklaus Design. Pinehills Golf Club offers the most extensive practice facilities in New England and three golf schools providing quality PGA instruction.

Cost is $125 per person before October 3, 2003, and $150 per person after.

The cost includes: Round trip Coach Transportation to Links, Greens Fees, Choice of Course (2), Personalized Bag Tags, Golf Carts, Locker Rooms, Unlimited Range Balls, Scoring by a PGA Professional, Bag Drop Service, and LUNCH.

**PLEASE NOTE:** Proper golf attire is required. Men’s shirts without collars, gym shorts, and jeans are not permitted. The Golf Course also requires that all players wear soft-spiked golf shoes.

Hole sponsorships are available: $400 & $600. Please contact Doug Paul, (dpaul@imaps.org), IMAPS HQ for details.

**Hole Sponsor:**
Presidio Components, Inc.
student program

Students, you are cordially invited to attend the 36th International Symposium on Microelectronics. We’ve got exciting activities lined-up from November 16 - 20, 2003, and you will enjoy the culture and hospitality of the Boston area.

**Reduced Symposium Registration**
Students’ cost to attend the Full Technical Symposium is $10 for IMAPS student members and $15 for nonmembers (on or before October 3, 2003): $20.00 for members and $25.00 for non-members after October 3rd.

**Student Plant Tour**
On Tuesday morning students will take a bus and head for Corning IntelliSense in Wilmington, MA, to visit its MEMS fabrication and packaging facilities. The tour includes an Introduction & Overview of the company, MEMS fabrication facility tour, software presentation and demonstration of IntelliSuite CAD for MEMS, and the tour of MEMS packaging and assembly.

**Student Chapter Booth Competition**
Each student chapter is encouraged to enter a booth and exhibit on the main floor. These booths are free to student chapters and allow chapters to demonstrate their activities to the microelectronics industry. Chapters will be evaluated, by a panel of judges, on various criteria including. Recognition will be given to the Best Student Chapter Booth at the Student/Industry Reception that evening.

**Student Industry Panel/Reception**
The Student Industry Panel is your chance to learn career development insights from top-level industry professionals. The panel will be conducted on Tuesday afternoon from 3:00 pm - 4:30 pm. Professionals from the electronics and optical networking equipment industries, industry recruiters, and engineering educators will describe and discuss how their education, interests and career experiences led to their current positions. Students will also learn current industry expectations and what they should be doing now for their long-term career development. A Reception will immediately follow where students will have the opportunity to network one on one with the industry panelists and each other. Refreshments will be served.

**Professional Development Course (PDC) Monitor**
Students have the opportunity to serve as PDC Monitors. One student monitor will be assigned to each of the 18 PDCs during the Symposium. Course monitors will assist the PDC Instructors (distribute handouts, monitor lights, collect evaluations, etc.). Although the monitors will receive no financial compensation, they will receive all handouts and slides presented during the course. Monitors are assigned on a first-come, first-served basis. So, sign up early to get the PDC of your choice by emailing Angie Johnson, ajohnson@imaps.org, with your top 3 choices.

**Student Marketing Competition**
The IMAPS Symposium Committee is sponsoring the 2nd Annual Student Chapter Marketing Competition for the IMAPS 2003 Symposium. The competition focuses on packaging for several selected industry groups including automotive, wireless, optoelectronics, RF/microwave, RF/wireless and security systems. Students from participating universities are expected to develop the following three components for their competition: 1. A Marketing Plan; 2. Print Media Advertisements; 3. Electronic Media Advertising. The winning student chapter in each area will be announced at IMAPS 2003.

**Best Student Paper**
A review committee will attend all technical presentations by student authors to evaluate and determine the Best Student Paper. Student papers will be evaluated on technical knowledge, presentation skills, written manuscript, and audience interaction. The winning student will receive a certificate and recognition in the magazine Advancing Microelectronics.

**Employment Center**
The IMAPS Employment Center will be open Tuesday, November 18th – Thursday, November 20th. Here, students will be able to speak with different employers about job openings, and interview rooms will be provided if needed.

**Student Chapter President Meeting**
Student chapter presidents from the various universities will conduct their first annual meeting. This meeting will contain discussions on effective member recruiting methods and various other topics concerning the growth of student involvement in IMAPS. This will also be an opportunity for students from different universities to get to know the other student chapter presidents.
2002 - 2003
Sidney J. Stein Educational Foundation Graduate Grant Recipients

Donald Plumlee, Boise State University
Student Advisor: Amy J. Moll, Ph.D.
Paper title: Lab in a Package: Integration of Microfluidics and Sensors in LTCC Materials

Jing Lee, University of Kentucky
Student Advisor: Dr. Janet K. Lumpp
Paper title: Carbon Nanotube Filled Conductive Adhesives

Michael Folk, University of Arkansas
Student Advisor: Fred D. Barlow III, Ph.D.
Paper title: Characterization and Modeling of Embedded Passives in Low-Temperature Co-Fired Ceramic

IMAPS 2003 Sponsors
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Thanks!

IMAPS Awards Ceremony
Tuesday, November 18, 2003
11:40 AM - 12:15 PM
Hynes Convention Center

Daniel C. Hughes, Jr. Award
William D. Ashman Award
Corporate Recognition Award
John A. Wagnon, Jr. Technical Achievement Award
IMAPS Fellow of the Society
International Award
Best Paper - IMAPS 2002

Come say “Thanks” to those who contributed so much to IMAPS over many years. ALL WELCOME!
Historic Plymouth

Travel to Plymouth, America’s first permanent settlement, along Plymouth’s historic waterfront, view Plymouth Rock before boarding the Mayflower II, a full-size replica of the ship that carried the Pilgrims to the New World. Upon arrival at Plymouth Plantation, take a self-guided tour of the 1627 Village and Indian campsite. As you step back in time, “interpreters” make the 17th century come alive. Then, enjoy a traditional 17th century luncheon that includes sampling of English and Wampnoag dishes.


The North Shore: Seaside Villages

A short distance from Boston you will find some of New England’s most picturesque seaside villages. Experience the uniqueness of Marblehead, the racing yacht capital of the world. Marvel at the breathtaking views of the Atlantic Ocean and the rocky coastline at Castle Rock on Marblehead Neck. Wind through Old Town to view period homes of the 17th and 18th centuries. In Salem, learn about the importance the maritime industry once had, and the infamous witch trials of 1692 as you tour through this period community. Enjoy a guided tour of the House of the Seven Gables, the home that was the inspiration for Nathaniel Hawthorne’s classic tale before a group luncheon at the historic Hawthorne Hotel. After lunch, there will be time on your own to stroll among the shops at Pickering Warf, or you may choose to visit the Salem Witch Museum or Peabody & Essex Museum which houses a vast collection of art and antiques from the China Trade.

Includes: Deluxe motor coach Transportation, Narration by Professional Tour Guide, admission at the House of Seven Gables, Luncheon.

Tuesday & Wednesday only: $200 – Advance; $250 – On-site.

Register on page 38.

PLEASE NOTE:

Buses will depart from the Dalton Street Entrance of the Sheraton Boston Hotel.
Tours will involve walking and participants should dress accordingly.
Comfortable walking shoes and layered clothing are recommended.

Spouse Program sponsored by:

Kester Solder - Northrop Grumman
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EXHIBIT AT IMAPS 2003
36th International Symposium on Microelectronics
November 16-20, 2003 * Hynes Convention Center * Boston, Massachusetts

IMAPS 2003 Exhibit Space
Still Available

Washington, D.C. - The International Microelectronics And Packaging Society (IMAPS) announces that limited Exhibit Space is available for the 36th Annual International Symposium on Microelectronics to be held November 16-20, 2003, at the Hynes Convention Center, in Boston, Massachusetts.

“We are extremely encouraged by the response our IMAPS Boston 2003 Symposium has received from the companies who have reserved a booth space,” stated Delip “Doug” Bokil, General Chair of IMAPS 2003. “This response proves that, although the economic conditions in our industry could be better, companies know that an IMAPS Symposium in the Boston area always brings in the customers they are seeking,” he further stated.

A current list of exhibitors can be found on page 39 of this advance program.

Act Fast - Space is Limited!

Reasons to Exhibit at IMAPS 2003

* IMAPS 2003 is the world’s largest symposium and exhibition devoted to the microelectronics/packaging industry.

* IMAPS 2003 will feature a powerful technical program, progressive professional development courses and many opportunities to share and learn about the latest technology developments.

* The last two IMAPS Symposia in Boston - ISHM 1994 & IMAPS 2000 - attracted, on average, more than 5,000 attendees.

* Ability to reach a large group of microelectronic packaging professionals all under one roof.

* Keep your company name in the eyes of your peers and customers.

* The Boston 2003 Committee is working with exhibitors to present a “Manufacturers’ Demonstration Line” (Demo Line) in the Exhibit Hall. The Demo Line will show new assembly technology used to manufacture a product from start to finish.

* IMAPS 2003 is also providing a presentation format to illuminate the latest assembly and packaging advancements. “Exhibitor State-of-the-Art Presentations” (ESAP), will give exhibiting companies a 15-20 minute session to present whatever products and services they deem important for the assembled audience. These sessions will be held during all exhibit hall hours.

* Your competition WILL be there!

* The greater Boston area contains the highest concentration of technology companies in North America.

To learn more or to register for a booth, visit www.imaps2003.org or contact Doug Paul, IMAPS HQ at 202-548-8712 or dpaul@imaps.org
The hands-on workshops sell out quickly and enrollment is limited, please check for availability.
Email Rayma Gollopp (rgollopp@imaps.org) or call 202-548-4001 ext. 711

Sunday, November 16
9 am - 5 pm

The “hands-on” courses are back! In the past the “hands-on” courses have sold out early and were an overwhelming success. IMAPS, in partnership with the National Training Center for Microelectronics (NTCμ) is again offering technical training sessions designed to provide attendees with a “hands-on” learning experience. Enroll early as class size is limited!

S1
Screen Printing (how to) for Operators and Technicians

CANCELLED
The National Training Center for Microelectronics (NTCμ), located in Bethlehem, Pennsylvania, is an extension of Northampton Community College. NTCμ is the recognized leader in microelectronics manufacturing industry training and is known for clear, concise “hands-on” training courses specializing in hybrid, RF and related technologies. All courses carry Continuing Education Units (CEU) which earn credit toward your degree. Website: www.northampton.edu/ntc.

S2
Wirebonding (how to) for Operators and Technicians

Enrollment limited to 10 students

Instructor: Thomas J. Green, National Training Center for Microelectronics

Workshop Summary:

This course is intended as a practical “hands-on” set of laboratory exercises to allow the operators to really understand the wire bonding process. An experienced industry instructor will review the basic manual wire bonder equipment design and setup and explore how machine settings such as power, time, force and stage temperature affect the bonding process. Both ultrasonic wedge and thermosonic ball bonding will be explored using the industry’s latest manual wire bonders. Students will also have an opportunity to perform wire pull and ball shear testing and visually inspect wire bond interconnects to gain further insights into the process.

What you will learn:

After completing the course, you will be able to:

- understand the basics of thermosonic and ultrasonic wire bonding
- recognize visual defects and how to prevent them
- learn how to do wire pull and ball shear testing
- know how to set up and use manual wirebonding equipment

Who Should Attend:

This course is intended as a beginning to intermediate level course for operators, technicians and others with limited wire bonding experience interested in a practical “hands-on” tutorial.

Tom Green has eighteen years experience in the microelectronics industry and presently teaches at the National Training Center for Microelectronics. As a staff engineer with Lockheed Martin he was responsible for the materials and processes used in building custom hybrids and RF microcircuits for space applications. Specific areas of expertise included wire bonding, die attach and seam sealing. As an officer assigned to USAF Rome Laboratories he conducted research on semiconductor failure mechanisms and analyzed numerous microelectronic component failures from Air Force avionics systems. He has published seven technical papers and is a member of the IMAPS National Technical Committee. Tom earned a B.S. in Metallurgy and Materials Engineering from Lehigh University and a Masters in Engineering from University of Utah.
Do you want to broaden and strengthen your skills and knowledge, optimize your manufacturing processes, and integrate the latest advances in materials and technologies to maintain your strength in today’s competitive global market? The Technical Committee of IMAPS is pleased to present a comprehensive offering of professional development courses that provide detailed information on topics of immediate interest to the Microelectronics and Packaging community. So please be sure to choose from the fifteen full day and two half-day in-depth technical workshops taught by recognized industry experts. You will discover the following key ways you will benefit...

- Better understand the industry’s fundamental skills and knowledge.
- Be exposed to the rapidly expanding developments in new materials and technologies.
- Consult with renowned authorities about your current R&D or manufacturing problems and challenges.
- Learn new ways to identify, think about, and address your problems and opportunities.
- Great opportunities to interact with industry experts and other course attendees.
- Certificate of Attendance and much more...

**Included in Your PDC Registration Fee:**

- Lunch on the day of your course
- Refreshment breaks
- All course materials
- PDC Reception on Sunday evening (for Attendees & Instructors only)
- Certificate of Attendance

**PDC CANCELLATION POLICY**

IMAPS reserves the right to cancel a course if the number of attendees is not sufficient. We shall then refund you the corresponding amount.

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**S3**

**Flip Chip and CSP Technologies – Constructions, Materials, Assembly and Reliability**

**Course Leader:**

R. Wayne Johnson, Ph.D., Auburn University

**Course Description:**

The increasing number of I/O per semiconductor chip combined with the product driven requirements of thinner, smaller and lighter weight have lead the electronics packaging and assembly industry to chip scale packages and flip chip (Flip Chip in Package (FCIP)) and Flip Chip on Laminate (FCoL) technologies. In fact, many CSPs use FCIP constructions. This course will begin by examining the drivers for flip chip and CSP technology concept will be explored. The replacement of leads by solder spheres impacts reliability, particularly in thermal cycling and bending, and must be considered prior to implementing these technologies. The course will conclude with a discussion of reliability.

**Who should attend?**

This Course is intended for those individuals soon to be responsible for implementing flip chip assembly, suppliers of materials and equipment for flip chip assembly and others interested in flip chip implementation.

Dr. Johnson is an Alumni Professor of Electrical Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). At Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and reliability for electronics assembly. He has worked in MCM design, MCM-L, C and D substrate technology as well as advanced SMT, wire bond and flip chip assembly techniques. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written two book chapters in the areas of silicon MCM technology and MCM assembly. He received the 1997 Auburn Alumni Engineering Council Senior Faculty Research Award for his work in electronics packaging and assembly. Dr. Johnson is the current Technical Vice President of IMAPS and was the 1991 President of the Society. He received the 1993 John A. Wagner, Jr. Technical Achievement Award from ISHM, was named a Fellow of the Society in 1994 and received the Daniel C. Hughes Memorial Award in 1997. He is also a member of IEEE, SMTA, and IPC. Dr. Johnson received the B.S. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering. He has worked in the microelectronics industry for DuPont, Eaton, and Amperex.
S4
Low Temperature Co-fired Ceramics (LTCC)
Course Leaders:
Fred D. Barlow and Aicha Elshabini, University of Arkansas

Course Description:
This course is a one-day PDC focusing on the materials, processes, design, and applications of Low Temperature Co-fired Ceramics (LTCC). The course will begin with a brief history and background of the technology. A detailed discussion of the process flow and processes will cover each step used in the fabrication of LTCC substrates. A discussion of the material properties and design guidelines and considerations will also be covered in detail. Finally, a discussion of the technical advances and the technical applications of the technology will outline the relative strengths of LTCC for a number of target markets.

Topics:
- History of LTCC and Background
- LTCC Process
- Material Properties
- Design Considerations
- Technical Advances
- Applications

Who should attend?
Engineers, managers, and technicians, who desire to expand their background or strengthen their understanding of the technology. The course will not assume any prerequisite background.

Aicha Elshabini is Professor of Electrical and Computer Engineering. She obtained a B.Sc. in Electrical Engineering at Cairo University, 1973, in both Electronics and Communications areas, a Masters in Electrical Engineering at University of Toledo, 1975, in Microelectronics, and a Ph.D. Degree in Electrical Engineering at the University of Colorado, 1978 in Semiconductor Devices and Microelectronics. Currently, she is serving the position of Professor and Department Head for the Electrical Engineering Department at University of Arkansas (since July 1, 1999), and Interim Department Head for Computer Science & Computer Engineering Department (since July 1, 2000). She has been serving as the faculty advisor for IMAPS student society at both institutions since 1980 to present time. Elshabini is a Fellow member of IEEE/CPMT Society (1993), Citation for ‘Contribution to Hybrid Microelectronics Education and to Hybrid Microelectronics to Microwave Applications’, a Fellow member of IMAPS Society (1993), The International Microelectronics and Packaging Society, Citation for ‘Continuous Contribution to Microelectronics and Microelectronics Industries for numerous years’, Dr. Elshabini was awarded the 1996 John A. Wagonon Jr. Technical Achievement Award from IMAPS. She has served as the Editor of the IMAPS International Journal of Microcircuits & Electronic Packaging for 10 years.

Fred Barlow earned a Bachelors of Science in Physics and Applied Physics from Emory University in 1990, a Masters of Science in Electrical Engineering from Virginia Tech in 1994, and a Ph.D. in Electrical Engineering from Virginia Tech in 1999. He is currently working as Assistant Professor in the Electrical Engineering Department at University of Arkansas. Dr. Barlow has published widely on electronic packaging and electronic materials evaluation and is Co-Editor of The Handbook of Thin Film Technology (McGraw Hill, 1998). In addition, he has written several book chapters including two chapters on thin films and one on components and devices. He has achieved the Outstanding Contributions Award with IMAPS in recognition of his efforts in developing and implementing the CD-ROM project for IMAPS publications, IMAPS home page on the Internet, and for his technical contributions. He currently serves on the IMAPS national technical committee for power packaging. His research interests include electronic packaging for power electronic and microwave applications as well as RF and microwave design.

S5
Fundamentals of Fabrication and Packaging of MEMS, Related Micro and Nano Systems
Course Leader:
Ajay P. Malshe, Ph.D., High Density Electronics Center (HiDEC), University of Arkansas

Course Description:
Fabrication and application specific packaging of micro electromechanical systems (MEMS) is a subject of immense interest. Application of MEMS to existing products as well as for adding value / functions to the existing products. Particularly, key words, namely MEMS, micro systems and nano technology, have the captured attention of technology leaders. MEMS and related micro systems are typically divided into two application areas: sensors and actuators. These are applied for a range of applications such as automotive, biomedical, optical, RF, etc. Examples of systems, devices and related application specific packages, are accelerometers, gyro's, DMD, lab-on-a-chip, SMART drugs, etc. Further, with the major investment and key advancements in nanotechnology, nano integrated MEMS and related micro devices and packages are of major importance to the next generation of engineered electronic systems.

Course Notes:
(1) Chapter by “Packaging of MEMS and MOEMS: Challenges and A Case Study” by Drs. Malshe and O’Conner, (2) copies of the transparencies on MEMS and Nanomanufacturing, and (3) publication “NSF-EC Workshop on Nanomanufacturing and Processing: A Summary Report,” Malshe et al., SPIE International Symposium on Smart Materials, Nano-, and Micro-Smart Systems, Melbourne, Australia, December 2002.
Specific Topics Covered:


Afternoon Session (Module II): An Introduction to M4 and MEMS, their Packaging and Assembly, and Nano Packaging and Manufacturing.

Who should attend?

The course is meant for industry and academic leaders and investors in science and engineering with interest in MEMS and related micro and nano systems. Highly recommended for R&D scientists, engineers and managers involved in sensors, actuators, instrumentation and systems related to micro and nano systems technology. Graduate students with special interest in the above areas will also find it useful.

Ajay P. Malshe is an Associate Professor at the Department of Mechanical Engineering, Director of SERC for Durable Micro and Nano Systems, and an adjunct faculty at the High Density Electronics Center (HiDEC), Department of Electrical Engineering, University of Arkansas, USA. His three distinct fields of research and educational interest are integration and advanced packaging of micro and nano systems, nanomanufacturing, and surface engineering of materials for advanced manufacturing. He has edited two proceedings, and authored two book chapters including one on MEMS Packaging; over one hundred referred publications, holds five patents and four pending. He is currently an active Executive Council member of International Microelectronics And Packaging Society (IMAPS) through the organization of Advanced Technology Workshops (ATW) on MEMS Packaging. Currently, he is Chairman of Thermal Management Technical Subcommittee and also National Chair of Topical Technology Workshops for IMAPS. In addition he is an active member of ASME, IEEE, MRS and AVS.

S6 Advanced Organic Substrate Package Design & Manufacturing for RF & Broadband Applications

Course Leader: Hassan Hashemi, Conexant Systems

Course Description:

The objectives of this course are to review design and manufacturing practices and tradeoffs affecting current and next generation RF & GHz Packaging using laminate substrate technologies in single or multiple die packaging format. The course material is primarily based upon the instructor’s experience on current practices used for Wireless & GHz IC packaging for internet infrastructure applications. The course is designed for engineers or engineering managers who want to understand more about laminate single or multi chip modules, and the unique requirements for assuring that packages can be manufactured in a high volume commercial application and meet stringent electrical and thermal performance requirements.

Course Content:

- Overview of Multi Chip packages and their benefits
- Review RF laminate packages designed to use Chip On Board, embedded passives, & SMD
- RF MCM-L design issues with emphasis on design for high volume manufacturing
- Power Amplifier modules, Transmit modules, and Radio-on-a-Package modules
- Package electrical, thermal, and mechanical modeling in support of design verification and process development
- Review of MCM-L materials, processes, and manufacturing issues
- Discuss quality and reliability concerns with RF MCM-Ls

Who should attend?

The course is intended for both the packaging expert (Electrical and Mechanical Engineers) as well as persons new to the field. The course will concentrate on extending the existing organic substrate infrastructure capability to GHz high volume packaging applications. The information presented will include the theoretical background with practical methods for implementing a design. These same techniques can be applied to other high frequency single or multichip package designs.

Hassan Hashemi is Executive Director of Advanced Packaging & Product Development at Mindspeed Technologies, a Conexant Systems Business in Newport Beach, California. He is currently managing design and development of single and multi-chip packages for broadband digital, mixed-signal, and RF devices used in infrastructure communication and storage applications. He holds a Masters degree in electrical engineering from the University of Texas at Austin, and has over 18 years of experience in microelectronics design, packaging, manufacturing, and product development. Prior to joining Conexant, he was a senior member technical staff at Microelectronics and Computer Corp. and Advanced Micro Devices. He holds 14 US patents, has authored three book chapters and over 40 technical papers in the areas of high-speed package electrical and thermal design and implementation.

S7 RF/Microwave Hybrids: Basics, Materials and Processes


Course Description:

In recent years, the demands for high frequency systems and products have been growing at a rapid pace. Coupled with the continuing development of monolithic integrated circuits, MMICs, are new materials and process refinement of hybrids. As a result, system and product designers are faced with the choice between hybrids and MMICs; i.e., complete system on a chip vs. hybrids with discrete devices, or more often, somewhere in-between. This course will begin with a short, non-mathematical review of high frequency basics. Next a comparison of MMICs and hybrids is presented. The
transmission line as the basic circuit component of RF and microwave hybrids will be reviewed. Hybrid “waveguide” structures will be compared as they relate to transmission line properties. The basic materials (conductors, dielectrics and substrates) and their properties will be introduced. Their effect on impedance, circuit properties and performance will be discussed. Processing technologies suitable for RF/microwave hybrids will be reviewed. Selected packaging protocols, such as vias and bonding wires, will be discussed in light of their influence on RF/microwave performance. At the completion of this course, attendees will have a better understanding of many of the critical materials and processing factors affecting high frequency circuit performance.

Who should attend?

This introductory course will benefit those associated with the RF and microwave arena. In particular this course will benefit those with responsibility for design and manufacturing of RF/microwave hybrids. Supervisors, engineers and technicians involved in product development, design and manufacture are encouraged to attend.

Special Course Materials:

All attendees will receive a set of course notes and a copy of the Mr. Brown’s text “RF/Microwave Hybrids: Basics, Materials and Processes.”

Special Course Materials:

All attendees will receive a textbook entitled: “Ball Grid Array and Fine Pitch Peripheral Interconnections,” published by Electrochemical Publications, LTD, Great Britain, (List Price US$149) and a workbook.

Who should attend?

This capsule view will provide attendees in managerial, marketing, engineering and research capacity a broad understanding of the industry as well as the quick grasp of the technological thrusts.

Dr. Hwang received her doctorate in Materials Science & Engineering from Case Western Reserve University and two masters from Columbia University and Kent State University’s Liquid Crystal Institute. She has been a major contributor to Surface Mount Technology since its inception. Serving as an advisor to major OEMs/ODMs, U.S. government and contract manufacturers, she has provided solutions to many challenging production-floor problems in the last 20 years of SMT establishment, including U.S. F-22 program. Among her many honors and awards, Dr. Hwang is elected to the National Academy of Engineering, inducted to the WIT International Hall of Fame, and received Distinguished Alumni Award from her alma maters. She also received the U.S. Congressional Certificate of Recognition, YWCA Women of Achievement Award, and was named one of the 28 R&D-Stars-to-Watch by Industry Week. She has held various “Woman pioneering” capacities. She is an invited lecturer/keynote speaker worldwide and the author of over 200 publications, including the sole authorship of five internationally used textbooks and a co-author of several books related to electronic packaging and assembly technologies. She writes a monthly column for SMT Magazine. Contributing to corporate governance, education and community, Dr. Hwang has served on various corporate, educational, and civic boards. She is a member of various professional organizations, having served as the National President of Surface Mount Technology Association. She has held executive positions with Lockheed Martin, SCM and IEM Corp., currently the president of H-Technologies Group Inc., providing technology and business solutions to the electronics industry.

Information technology involves hardware, software, applications and services. This industry has become the largest industry surpassing agriculture that lasted more than a millennium and steel that lasted more than a century. It is becoming the driving engine for science, technology, manufacturing and services paving the way for unparalleled prosperity of people and countries that participate in it. Better than 80% of all millionaires in the U.S. during the last five years have been attributed to this industry.

Microelectronics systems packaging involves all the technologies in forming electronic systems for consumer, telecom, computer, automotive, aerospace and medical industries. These technologies typically involve all the components and their interconnections to form system level boards to provide system level functions. Microelectronics packaging is the ultimate cross-disciplinary technology that involves engineers from various backgrounds. For example: electrical design typically performed by Electrical or Electronic and Computer Engineers; thermo-mechanical design by Mechanical Engineers; development of new materials that provide the required functions by Materials Engineers; fabrication of components by Chemical Engineers; electrical test by Electrical or Electronic Engineers; IC and board assembly by Mechanical or Materials Engineers; thermal management and reliability by Mechanical Engineers; and so on. Working together as a team from all these disciplines, packaging engineers design, fabricate, integrate, test, cool and assure reliability of the entire microelectronic system.

This four-hour course will present the global microelectronics market, past and future technologies that constitute this market, the educational opportunities that are available and career prospects for a lifelong career around the world in various industries.
professional development courses


M1
Packaging Challenges and Solutions for 10 Gb/s and 40 Gb/s Systems
Course Leaders:
Roberto Coccioli and Hassan Hashemi, Inphi Corporation and Conexant Systems

Course Description:
The objectives of this course are to review challenges in 10G and 40G IC packaging considering requirements posed by mixed IC technologies and system architecture. Moreover, it is intended to review the technologies available to realize package and board interconnects assessing their relative performance and their impact on signal integrity on high speed digital signaling. The course material is based upon the instructors’ experience on current practices used for GHz IC packaging for telecom, datacom, and storage infrastructure applications. The course is designed for engineers or engineering managers who want to understand more about technical challenges of high-speed packaging and the unique requirements posed on technology selection and design to assure the achievement of stringent electrical and thermal performance in cost-performance efficient manufacturing.

Who should attend?
The course is intended for both the packaging expert (Electrical and Mechanical Engineers) as well as persons new to the field. The course will review the existing substrate infrastructure capability and explore ways to extend its use to high volume packaging of ICs for telecom, storage, and datacom applications. The information presented will include the theoretical background with practical methods for implementing a design. These same techniques can be applied to other high frequency single or multichip designs.

Roberto Coccioli is Senior Design Engineer at Inphi Corporation, Westlake Village, CA, where he is currently working on development of ceramic and metal packages for GaAs and InP ICs for 10Gbps and 40Gbps systems. Prior to joining Inphi, he was a design engineer at Conexant Systems, Inc, Newport Beach, CA, where he worked on modeling, design and characterization of high-density organic and ceramic packages for Si and GaAs ICs for high-speed digital communications, organic packages for RFICs, and embedded antennas. Coccioli holds a Ph.D in Electrical Engineering from the University of Florence, Italy, and has been Visiting Scholar and Postdoctoral Fellow at UCLA from 1996 to 1999, where his research focused on numerical methods for electromagnetics and its applications to the analysis of microwave passive and active circuits, antennas, and photonic bandgap materials. He holds 1 US patent, has co-authored one book, and over 25 papers in the area of microwave and electromagnetic modeling. Roberto Coccioli is a member of IEEE.

M2 - CANCELLED
Process Engineering Fundamentals
Course Leader:
Thomas J Green, National Training Center for Microelectronics

Course Description:
The objective of this course is to teach the fundamental process engineering tools and techniques needed for the microelectronics packaging industry. The focus of this course is to provide an overview of the skill sets required to effectively control and optimize a microelectronics manufacturing process flow. The course begins with a review of the common materials and manufacturing processes used in the hybrid microelectronics industry including common assembly processes for RF MMIC modules and optoelectronic devices. Basic manufacturing processes such as thick and thin film fabrication, die attach, wire bond and hermetic seal are reviewed from a materials and processing standpoint. Next, process characterization and statistical methodologies are introduced with a focus on practical applications. The basic concepts of Design of Experiments (DOE) including set up and analysis of a simple industry fractional factorial experiment is covered. Statistical Process Control (SPC) techniques and sample charts are also reviewed with a special emphasis on Cp and Cpk calculations. Finally, industry accepted Defect Recognition and Workmanship Standards are presented.

Knowing what to look for and how the visual defects relate to the process is critical from a quality, reliability and yield perspective. Clear color photos of excessive probe marks, chip outs, air bridge damage, die at-
tach and wire bond defects along with numerous other defects will be presented to the class and discussed in detail. The last segment of the course is an overview of the analytical tools and techniques available to process engineers for failure cause investigation and as tools in process optimization projects.

Who should attend?

This PDC is intended as an introductory to intermediate level course for process engineers, designers, quality engineers, and experienced technicians responsible for microelectronics materials and process development and manufacturing process improvements.

Tom is an independent consultant and adjunct professor at the National Training Center for Microelectronics. At NTCM he designs curriculum and teaches industry short courses relating to advanced microelectronics manufacturing processes. He has over twenty years experience in the microelectronics industry at Lockheed Martin Astro Space and USAF Rome Laboratories. During that time period he was a staff engineer responsible for the materials and manufacturing processes used in building custom high reliability space qualified microcircuits (Hybrids, MCMs and RF modules) for military and commercial communication satellites. Tom has demonstrated expertise in wire bonding, component attach, and seal sealing processes. He has conducted and analyzed numerous statistically designed experiments, which increased first pass yield, reduced costs and improved product quality. At Rome Labs he worked as a senior reliability engineer and analyzed component failures from AF avionics equipment. Tom is an active member of IMAPS at both the regional and national level. He has published seven technical papers and is a member of the IMAPS National Technical Program Committee and Optoelectronics sub committee chair. Tom earned a B.S. in Metallurgy and Materials Engineering from Lehigh University and a Masters in Engineering from University of Utah.

M3 Advanced Materials for Microelectronic, Optoelectronic and MEMS/MOEMS Packaging and Thermal Management

Course Leader:
Dr. Carl Zweben, Advanced Packaging Materials and Composites Consultant

Course Description:

Materials impact performance, reliability, manufacturing yield and cost. Increasingly, traditional packaging materials are failing to meet the requirements of new microelectronics, optoelectronic and MEMS/MOEMS packaging designs. In response, numerous advanced composites and monolithic materials have been, and are continuing to be developed. Property improvements include: thermal conductivities ranging from extremely high (over 4X copper) to very low; low, tailorable coefficients of thermal expansion; electrical resistivities ranging from very low to very high; extremely high strengths and stiffnesses; low densities; and low cost. Net shape fabrication processes. A new thermal interface material has a reported thermal conductivity of 750 W/m.K. Payoffs include: improved thermal performance; reduced thermal stresses and warpage; improved fiber alignment; simplified thermal design; possible elimination of thermal interface materials; liquid cooling and heat pipes; weight savings up to 85%; size reductions up to 65%; increased reliability; reduced electromagnetic radiation emissions; increased manufacturing yield; and potential cost reductions.

Advanced materials, such as Al/SiC metal matrix composites (first used in packaging by the course leader) and carbon fiber-reinforced polymer matrix composites, are now being used in a growing number of high volume commercial and aerospace production applications at the rate of millions of piece parts annually. Components include heat spreaders, microprocessor heat sinks, air-cooled and liquid-cooled cold plates, microwave modules, power semiconductor modules, optoelectronic packages, and heat pipe over molds. Products using these materials include servers, cellular telephone handsets and base stations, laptop computers, hybrid and electric vehicles, trains, wind tur-
M4 - CANCELLED
Fiber Optics Structures: Design for Reliability
Course Leader: E. Suhir, University of Illinois at Chicago and ERS Co.

Course Description:
In this course we determine the role of materials, structural attributes and loading conditions on the mechanical behavior and reliability of optical fiber interconnects, whether bare, polymer coated or metallized. The emphasis is on the predictive modeling and the analytical (“mathematical”), rather than numerical (FEA) approach.

What will you learn?
The course should enable you to:
- Use easy-to-apply formulas that consider the impact of the major materials and geometric factors on the state of stress and strain in, and the reliability of, optical silica fibers.
- Choose the appropriate material(s) for a particular design and decide how to change, if necessary, the geometrical characteristics of the design to create a viable and reliable fiber optic structure.
- Evaluate stresses and displacements (curvatures) in bare fibers, subjected to bending or to combined action of bending and tension, with consideration, if necessary, of the nonlinear stress-strain relationship of the silica material.
- Analyze the mechanical behavior of polymer coated or metallized fibers, experiencing tension, bending, or the combined action of bending and axial loading, as well as the interfacial strength and strippability of polymer coated fibers.
- Evaluate and prevent thermal stress-strain failures in fiber optics structures (examples include: bow-free assemblies and optical fibers soldered into ferrules), and to explain and evaluate the interaction of “global” and “local” thermally induced stresses in optical glass fibers adhesively bonded or soldered at the ends into ferrules or capillaries.
- Compute and analyze the elastic stability and microbending of optical fibers (low temperature microbending of long haul optical fibers, buckling of bare, polymer coated or metallized optical fiber interconnects with or without lateral and/or angular misalignments of their ends, etc.)
- Predict the dynamic response of fiber optic structures to shocks and vibrations, applied to their “supports”
- Get an insight into, and explain the role, attributes, challenges, and pitfalls of, the accelerated life testing of photonic systems and its interaction with the qualification (Telcordia) and product-development testing.

Who should attend?
Engineers and technical managers who encounter and have to solve various materials, mechanical and reliability problems in fiber optics engineering. Prior knowledge of stress-strain analysis and the elementary theory of bending of beams is desirable, but not required.
- Dr. Suhir is Distinguished Member of Technical Staff (ret.), Bell Laboratories, Basic Research Area, Physical Sciences and Engineering Research Division (1984-2001). He is currently Adjunct Professor, the University of Illinois, Chicago, IL. Dr. Suhir is Fellow of the American Physical Society (APS), Institute of Electrical and Electronics Engineers (IEEE), American Society of Mechanical Engineers (ASME), and the SPE (Society of Plastics Engineers). He is co-founder and technical editor of the ASME Journal of Electronic Packaging. Dr. Suhir has authored numerous technical publications (papers, book chapters, books, patents), including monographs "Structural Analysis of Microelectronic and Fiber Optic Systems," Van-Nostrand, 1991 and "Applied Probability for Engineers and Scientists," McGraw-Hill, 1997. He received numerous distinguished service and professional awards, including: 2001 IMAPS John A. Wagnon Jr., Technical Achievement Award, 2000 IEEE Outstanding Sustained Technical Contribution Award, 2000 SPE Fred O. Conley Award, and 1999 ASME and Pi-Tau-Sigma Charles Russ Richards Memorial Award. Dr. Suhir is a member of the IEEE Technical Advisory Board (TAB), Distinguished Lecturer of the IEEE CPMT (Components, Packaging and Manufacturing Technologies) Society and Member of the Board of Governors of this Society. He is also Member-at-Large of the IEEE Technical Advisory Board. Dr. Suhir presented numerous invited and keynote talks in universities and at professional conferences worldwide, and taught many professional development and university courses on various topics of materials, reliability and mechanical problems in micro-, opto-electronics and other areas of engineering and applied science.

M5 - CANCELLED
Die Products – Overcoming the Domination of Moore’s Law
Course Leader: Larry Gilg, Die Products Consortium

Course Description:
Semiconductor die products have evolved from the hybrid era of chip on board technologies to the stacked, SIP, and wafer-level CSP technologies at the leading edge of the microelectronics industry. Today’s advanced packaging technologies rely on expertise developed in the bare die business for testing, screening, packing, shipping, assembly technologies and standards. This full-day professional development course will cover vital technologies for practitioners in all phases of the advanced packaging and assembly industry, with a focus on using die products solutions to achieve smaller form factor, higher performance, and lower cost.

This course is the collaborative work of member companies of the Die Products Consortium (DPC). The DPC has been active in developing the infrastructure for the die products industry for the past 10 years, beginning as a project of SEMATECH and MCC throughout most of the 90s, and now as an independent consortium helping its members achieve success in die products markets in the new millennium.

What will you learn?
- Die Products Overview – Basic definitions, die products market trends, simplified discussion of die
products technology choices, and a “tear-down” analysis of a real product.

- Assembly Processes – Discussion of die preparation, inspection, shipping, handling, storage, bumping, under fill, encapsulation, and manufacturability.

- WL-CSP Technologies – Discussion of wafer level chip scale packaging technologies, including rationale, approaches, drivers, assembly considerations, and reliability evaluations.

- PCB Design Guidelines for Die Products – Overview of the tradeoffs required for interconnecting substrate design and development to achieve optimum assembly and ultimate reliability of die products modules.

- Die Products Standards – A detailed review of typical die data sheet to discuss requirements of die products standards such as IEC 62258.

- Die Products Supply Portfolio

- Die Products Roadmap

Who should attend?

This course will be beneficial to all managers and individual contributors from the electronic industry who need fundamental understanding and broad perspective on die and packaging of die requirements.

Larry Gilg is managing director of the Die Products Consortium, a collaborative effort among a group of microelectronics companies to enlarge the market for die products. Mr. Gilg has been active in the die products and Known Good Die (KGD) technology for the past 10 years. As a program manager at MCC, a R & D consortium for developing advanced packaging technologies, Mr. Gilg initiated, marketed and provided technical management of consortia and government sponsored programs for development of bare die assembly, test and reliability conditioning. In particular, the Die Products Consortium includes projects that evaluate wafer level test and reliability screens, develops standards and guidelines for die products, develops guidelines and tutorial information for users of die products, augments the infrastructure for KGD procurement and provides market intelligence and technical assessments to member companies.

In addition to these duties, Mr. Gilg has also: Led an industry task group to develop standards and guidelines for KGD, leading to adoption of JEDEC Standard No. 49, “Procurement Standard for Known Good Die.” Participated in SIA Assembly and Packaging Technology Working Group that developed the National Technology Roadmap for Semiconductors – 1997 & 1999 Editions. Developed symposia for audiences of technical professionals, including a full day tutorial on Known Good Die technologies presented at technical conferences over the past five years. Published several articles in the trade press and engineering journals, and authored a chapter on Known Good Die for the book, Flip Chip Technologies, edited by John Lau and published by McGraw-Hill in 1996. Authored chapter on Known Good Die Technology for the Wiley Encyclopedia of Electrical and Electronics Engineering, edited by John G. Webster, 1999. Founded and provides administration and program direction for the International KGD Packaging and Test Workshop, now in its 10th year, held in Napa, California. Larry Gilg is a Registered Professional Engineer in Texas and California.

M6 Wire Bonding in Microelectronics

Course Leader: George G. Harman, National Institute of Standards and Technology

Course Description:

Wire bond manufacturing defects range typically from about 1000 to 100 ppm, with exceptions to >10,000 and <50 ppm. In order to achieve the lower numbers in production, one must understand all of the conditions that affect both bond yield and reliability (since they are interrelated). This course will discuss many large- and small-wire bonding problems, as well as subjects of specific interest to hybrid/MCM device bonding. In addition, a number of advanced topics, such as high yield, fine pitch, and flex bonding will be covered. New developments (e.g., high frequency ultrasonic bonding), are included along with a major discussion of wire bonding to multichip modules and other soft substrates. Wire bond testing and metallurgy (covering both aluminum and gold bonds); intermetallic compounds; cleaning for yield and reliability; failures resulting from electroplating; mechanical problems in wire bonding; new bond technologies and developments; how ultrasonic bonds are formed, and the metallurgy of gold and aluminum wire. It concludes with methods of implementing TAB and Flip Chip by using wire bonding techniques.

Who should attend?

Engineers in R&D, QA, QC, manufacturing, process development, and advanced technicians. It is assumed that participants have some familiarity with wire bonding and general device assembly technologies.

Special Course Materials:

All attendees will receive a complimentary copy of Wire Bonding in Microelectronics, by George Harman, McGraw Hill, NY, 1997 (List price $65), as well as course notes and explanations.

Mr. Harman is a Fellow of the National Institute of Standards and Technology (NIST), Department of Commerce. He received a BS in Physics from Virginia Polytechnic Institute & State University and a MS in Physics from the University of Maryland. Mr. Harman has published 50+ papers, two books on wire bonding, and holds four U.S. Patents. He was the 1995 President of ISHM and is a Fellow of IMAPS and the IEEE. He has received numerous awards for his work from IMAPS, IEEE, DVS and others. He has presented numerous talks, and has taught courses for the University of Arizona and IMAPS for over 15 years, as well as the IEEE, to name a few. He has presented many papers and given courses in the USA, Europe, and Asia.

M7 Integrated Circuit Packaging Trends and Assembly Options

Course Leader: William J. Greig, Greig Associates

Course Description:

This course addresses the impact of both the Integrated Circuit, and End Product requirements (“smaller, better, cheaper”), on packaging, assembly, and substrate interconnects. It focuses on packaging trends, namely, the Ball Grid Array (BGA) and Chip Scale Package (CSP), Multichip Packaging (MCP) and alternative formats, Chip On Board (COB), and 3-D initiatives at both the chip and package levels. Assembly options available for attachment of the IC in each...
case will be discussed with major emphasis on Flip Chip. The course also covers the High Density Interconnect (HDIs) substrates. The various substrate technologies (Thick Film, Co-fired Ceramic, and Thin Film) that are employed in the manufacture of packages and component assemblies for MCPs will be reviewed. Finally, the latest developments in PWBs, with high density, fine lines, and micro vias employing sequential processing (Build Up Technology – BUT) will be reviewed. Throughout the course, technical issues will be emphasized and reliability concerns addressed where appropriate.

Special Course Materials:


Who should attend?

The course provides an overview of microelectronic packaging and assembly and is intended for individuals in any way involved with electronics manufacturing. While introductory in nature it discusses current status and future trends, it is directed towards both the experienced or inexperienced engineer and technician, and management personnel with the “need to know.” It should be of particular interest to those in support activities such as procurement, quality assurance, marketing and sales, and program office by providing a technology base in support of strategic planning and implementation.

Bill Greig is currently an independent consultant specializing in microelectronic packaging and assembly. His previous work experiences include RCA Semiconductor, General Electric Co., Lockheed Electronics, and NASA. His areas of expertise cover semiconductor wafer processing and assembly, hybrid circuit manufacture, and printed wiring board fabrication. He is experienced in assembly technologies such as chip & wire, TAB, and flip chip. He has been granted 6 patents and has published or presented numerous papers at the various technical symposia. He has developed and presented courses at national symposia and participated in CEE programs at U. of Wisconsin, Lehigh University and Rutgers University. He is a member of SMTA and IMAPS in which he is a Fellow, and Past President of the Garden State Chapter.

M8
Technology of Screen Printing
Course Leaders:
Art Dobie, SEFAR America & Rudy Bacher, DuPont

Course Description:

The purpose of this course is to increase the understanding of the screen printing process thereby improving production yield and quality. The critical and integrated components for screen, such as frames, screen mesh and emulsion are presented. Presented are some of the latest advancements in the screens, the compositions and the printing process that enable screen printing to meet future circuit density requirements. The course is applications-oriented in terms of how to optimize the screen printing process; how to specify and use screens; rheology properties that affect the print; minimizing printing defects and trouble-shooting problems related to the screens and the printing process.

Who should attend?

This course is intended for production and process engineers, and others interested in learning how to optimize and increase the uses of the screen printing process.

Art Dobie is Manager of Screen Technology for SEFAR America (MEC) in Mount Holly, NJ. He has been with MEC more than 22 years since receiving his BS in Screen Printing Technology in 1980 from California University of Pennsylvania’s School of Science and Technology. Art is an original instructor of IMAPS’ Technology of Screen Printing Professional Development Course, and has delivered many technical papers and presentations relating to screen printing technology to the microelectronics industry at the local, National and International levels. Art Dobie has held numerous offices in the Keystone Chapter, including president. Mr. Dobie was Co-Chair of Exhibits for ISHM ’97 and initiated the IMAPS Educational Foundation Silent Auction. Art is a Fellow of the Society of IMAPS and an inducted member of the Academy of Screen Printing Technology.

Rudy Bacher has worked 37 years in Thick Film Technology for DuPont Research and Development as a Ceramic Engineer and currently as a Development Associate. He is a recipient of the ISHM Technical Achievement Award-1984; Corporate Marketing Excellence Award-1994; and

M9
Lead-Free Electronic Packaging & Assembly: Technology and Manufacturing
Course Leader:
Dr. Jennie S. Hwang, H-Technologies Group, Inc.

Course Description:

Environment-friendly manufacturing and begin end-use products that are ultimately safe at the end of product life cycle is essential to technology-business competitiveness. This is a continuing challenge to the industry. Based on the newly released book: “Environment-Friendly Electronics—Lead Free Technology,” this course will cover all relevant topics and issues including global legislative status, technological base, material fundamentals, product assessment, cost, applications, processes and other manufacturing considerations. The viable lead-free solder alloys will be ranked in their key performance parameters to facilitate implementation. The courses will emphasis on practical applications in the SMT infrastructure including reflow and wave soldering. Information is applicable to all types of electronic packages and assemblies including QFP, BGA, flip chip and CSP.

What will you learn?

• Driving forces and industry trends
• Legislation status – US, Japan, Europe
• General introduction of role of lead and key illustrations
• Lead-free technology base
• Comparison of viable lead free alloys
• Alloys wetting vs. manufacturing performance in reflow & wave soldering
• Reflow criteria vs. PCB soldering
Dr. Hwang received her doctorate in Materials Science & Engineering from Case Western Reserve University and two masters from Columbia University and Kent State University’s Liquid Crystal Institute. She has been a major contributor to Surface Mount Technology since its inception. Serving as an advisor to major OEMs/ODMs, U.S. government and contract manufacturers, she has provided solutions to many challenging production-floor problems in the last 20 years of SMT establishment, including U.S. F-22 program. Among her many honors and awards, Dr. Hwang is elected to the National Academy of Engineering, inducted to the WIT International Hall of Fame, and received Distinguished Alumni Award from her alma maters. She also received the U.S. Congressional Certificate of Recognition, YWCA Women of Achievement Award, and was named one of the 28 R&D-Stars-to-Watch by Industry Week. She has held various “Woman Pioneering” capacities. She is an invited lecturer/keynote speaker worldwide and the author of over 200 publications, including the sole authorship of five internationally used textbooks and a co-author of several books related to electronic packaging and assembly technologies. She writes a monthly column for SMT Magazine. Contributing to corporate governance, education and community, Dr. Hwang has served on various corporate, educational, and civic boards. She is a member of various professional organizations, having served as the National President of Surface Mount Technology Association. She has held executive positions with Lockheed Martin, SCM and IEM Corp., currently the president of H-Technology Group Inc., providing technology and business solutions to the electronics industry.

Who should attend?

Managers, engineers, project managers, purchasing managers, sales and marketing personnel.

E. Jan Vardaman, President and Founder, TechSearch International, Inc., Austin, Texas. Ms. Vardaman analyzes international developments in the field of semiconductor packaging and assembly. Previously she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC) in Austin, Texas, where she analyzed international developments in semiconductor packaging and assembly. She is the editor of Surface Mount Technology: Recent Japanese Developments, published by IEEE. She is a columnist with Circuits Assembly magazine, and author of numerous publications on emerging trends in semiconductor packaging and assembly. She served on the NSF sponsored World Technology Evaluation Center (WTEC) study team involved in investigating electronics manufacturing in Asia and a U.S. Government study mission to China. She is a member of IEEE’s CPMT society Board of Governors and IMAPS. Ms. Vardaman received her B.A. in Economics and Business from Mercer University in 1979 and her M.A. in Economics from the University of Texas in 1981.

Special Course Materials:


Who should attend?

Management, engineers, technicians, project managers, purchasing managers, QA engineers, researchers and others involved in electronics materials, electronics manufacturing and decision-making in forming and implementing manufacturing strategies through a general understanding of lead-free solder and environment-friendly electronics manufacturing.

1/2 Day Course - PM
M10 runs 1 PM - 5 PM

Advanced Packaging Developments and Trends

Course Leader:
E. Jan Vardaman, TechSearch International, Inc.

Course Description:

The semiconductor industry has seen a major shift from leads to balls and from wires to bumps. This requires infrastructure developments and promises new opportunities. This course will cover developments and trends in area array packages. Ball grid array (BGA) packages are increasingly found in products including personal computers, portable communications devices, workstations, servers, mid-range and high-end computers, network and telecommunications systems, and even automotive applications. Package trends and new developments are described. Driven by the demand for smaller, lighter, thinner portable products has come the development of chip scale packages (CSPs). Discussed are the various types of CSPs in volume production and new developments such as wafer level packages. Flip chip’s advantage over wire bond interconnection includes higher density mounting, improved electrical performance, and improved reliability for many applications. New applications for flip chip are described. Also included are trends such as bump pitch, bump metallurgy, and substrate feature sizes.

What will you learn?

- Driving forces and industry trends
- New applications for BGAs and CSPs
- Wafer level packaging applications
- Flip chip applications
- New package constructions
- Pitch trends
- Lead-free developments and trends
- Infrastructure developments
- Substrate developments
- Underfill material and equipment developments
Back by Popular Demand!

The IMAPS 2003 Internet Cafe

IMAPS 2003 will offer the 2nd annual “IMAPS Internet Cafe” and there are Sponsorship opportunities available for this exciting high traffic area that will feature:

♦ Four PC stations with high-speed (Fiber) Internet Connection so attendees will be able to log on to the web and check email within seconds.
♦ A convenient location in the Convention Center adjacent to other high traffic areas.

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* OR, your company can be the sole Sponsor of the “IMAPS Internet Cafe” for $4,000.

Please call Doug Paul at 202-548-8712 or e-mail: dpaul@imaps.org if you have any questions or wish to sign-up as a Sponsor for the “IMAPS Internet Cafe.”

IMAPS Employment Center

Due to the success of the Employment Center at IMAPS 2002 in Denver, we have decided to sponsor the Employment Center at IMAPS 2003, 36th Annual Symposium on Microelectronics at the Hynes Convention Center in Boston, MA. Take advantage of this no fee service; it’s a great way to gain immediate face-to-face contact with potential employers/employees.

The Employment Center will post job openings, collect resumes, offer on-site interview space and help schedule interviews at the potential employer’s request. In addition, each resume if requested will be entered into the IMAPS JOBS Marketplace.

Employers need not be present to post job openings. Send us your job openings and we’ll collect resumes for you. Postings may be internships or anything from entry level to executive management. Company literature tables are available to promote your company to job applicants.

To submit job postings prior to Sunday, November 16, 2003; e-mail job descriptions to Silke Spiesshoefer (sspiess@uark.edu) or call 479-575-3967. After this date, please submit on site. You may also contact IMAPS Member Relations - Ann Bell at 202-548-8717 (abell@imaps.org) for more information.

Employment Center Hours (Open one half hour past exhibit hours):

Tuesday, November 18th:  9:00 a.m. –5:30 p.m.
Wednesday, November 19th:  9:00 a.m. –5:30 p.m.
Thursday, November 20th:  8:00 a.m. –12:30 p.m.
Advanced materials are a key element in microelectronics and packaging. The leading edge of materials development and application are reported, including Organic Electronics and OLEDs, LCPs, Opto-Electronic Packaging and NanoTechnology.

Organic Electronics: An Overview
Philip Garrou, David Brennan, Mitchell Dibbs, Paul Townsend, The Dow Chemical Company

Advances in Deposition of OLEP Materials via Piezoelectric Ink Jet
Linda T. Creagh, Marlene McDonald, Spectra, Inc.; Susanne Heun, Covion Organic Semiconductors GmbH; Neil Tallant, Aecia Ltd.

Polymeric Material Solutions and Performance Criteria for Jettable Fluid Delivery Assembly and Harsh Environment Protection
Susan Krawiec, Chih-Min Cheng, Robert Palmer, Emerson & Cuming

The Liquid Crystal Polymer Packaging Solution
Brian Farrell, Paul Jaynes, Foster Miller, Inc.; Wayne Johnson, Robert Dean, Auburn University

Epoxies for OptoElectronic Packaging: Applications and Material Properties
Michael J. Hodgin, Epoxy Technology, Inc.

Middle-Permittivity Dielectric Compositions for Functional LTCC Substrate
Young-Jin Choi, Jeong-Hyun Park, Jae-Hwan Park, Byung-Kook Kim, Jae-Gwan Park, Korea Institute of Science and Technology

Carbon Nanotube Filled Conductive Adhesives
Jing Li, Janet K. Lumpp, Eric Grulke, University of Kentucky

Fine Line Printing Technologies for Microwave and Millimeter Wave Applications

Novel Failure Mechanism Involving the Motion of Oxygen Vacancies in Chip Capacitors
Roy Tom Coyle, Jr., Northrup Grumman Space Technology

Thick-Film Initiators for Automotive Applications
Walter Smetana, Roland Reicher, Heinz Homolka, Vienna University of Technology

Cerium Oxide Based Screen-Printed Thick Film Components as Gamma Radiation Sensors
Khalil Arshak, Olga Korostynska, University of Limerick

Automotive Module Design using Self-Constrained Zero-Shrink LTCC
Frans Lautzenhiser, Randy Klein, Heraeus Inc.; Annette Kipka, Christina Modes, W.C. Heraeus GmbH & Co., KG

A Case Study of Lead Free Thick Film Conductors with Lead Free Solder Alloys
Theresa D. Sims, Peter Bokalo, Samson Shahbazi, Heraeus Inc., Circuit Materials Division

Performances of High Voltage Screen-Printed ZnO Varistors
M. P. Martin, H. Debéda-Hickel, C. Lucat, F. Ménil, P. Tardy, University of Bordeaux

Quality and Reliability of 100 µm Pitch Flip Chip ICs on Flexible Substrates with Adhesive Interconnections
J. de Vries, J. van Delft, C. Slob, Philips Center for Industrial Technology

A Study of Non-Flow Under-Fill Flip-Chip Bonding Process for LCP Based COF Components
Satoshi Furuki, Hiroyuki Takahashi, Chihiro Hatano, Makoto Yamasaki, Nippon Steel Chemical Co., Ltd.

A Comparison of Electromigration and Thermal Fatigue Performance Between Thin and Thick Film UBM

High-Performance Liquid Crystalline Polymer Printed Circuits
Katsufumi Hiraishi, Kazunori Ueda, Katsumi Takata, Isamu Takarabe, Nippon Steel Chemical Co., Ltd.

System Packaging for Robust LGA Interconnect Technology in High Performance Computing Applications
Mark K. Hoffmeyer, John L. Colbert, John G. Torok, John S. Corbin, William L. Brodsky, IBM Corporation

An Approach to Custom CSP Package Fabrication
Joseph W. Soucy, Henry G. Clausen, Charles E. Busa, Fredrick J. Kasparian, Draper Laboratory
Advanced Wirebonding
Chairs: Lee Levine, Kulicke & Soffa Ind. Inc.; Bruce Romenesko, The Johns Hopkins University/APL
8 am - 11 am
This session deals with the challenges encountered by wire bonding at fine pitch, low temperature and on copper/Low K dielectric surfaces.

Process Optimization for the 0.13 μm Cu / Low K (Black Diamond™) Dual Damascene Interconnection
Li Hongyu, Su Yong Jie, Tsang Chi Fo, Sohan Singh Mehta, Bliznetsov Vladimir, Zhang Lin, Institute of Microelectronics - Singapore

Impact Analysis of Wirebonding on Cu/Low-K Structures
Chang-Lin Yeh, Yi-Shao Lai, Jenq-Dah Wu, Advanced Semiconductor Engineering, Inc.

Gold Ball Bonding on Copper Substrates at Ambient Temperatures
I. Lum, N. J. Noolu, Y. Zhou, University of Waterloo

Optimization of Wire Bonding over Cu–Low K Pad Stack
P. Keller, J. W. Brunner, Kulicke & Soffa Ind., Inc.; T. Pan, Applied Materials

Morphology of Ball Bonds at <50µm Pitch
Lee Levine, Jon Brunner, Gary W. Schulze, Kulicke & Soffa Ind., Inc.

Dynamic Characterization of NiTiNOL for Interconnection Applications
Shivamanda Pai Mizar, Ryszard J. Pryputniewicz, Worcester Polytechnic Institute

Passive Integration in LTCC, PWB and On Chip
Chair: Robert H. Heistand II, AVX Corporation
8 am - 11:25 am
The integration of passive elements into substrates and packages continues to break new ground.
Examples of passive integration technologies, techniques and design attributes are presented for LTCC, PWB and on chip applications. The final paper compares LTCC and HDI organic technologies for RF applications.

A 5 to 6.5 GHz LTCC Power Amplifier Module
N. Ilkov, R. Matz, O. Demnovsek, Siemens AG; W. Bakalski, W. Simbürger, Infineon Technologies AG; P. Weger, Technical University of Brandenburg

Modeling and Analysis of LTCC Stripline for Multi-Layer Packaging
Jae Hyuk Jang, Seung Gyo Jeong, Byeung Gyu Chang, Ji Hwan Shin, Samsung Electronics Mechanics

Performance of Co-Fired Buried Resistors in A6S Tape
Michal Moroz, Ferro Corporation

Wafer Level Packaging Technology for Low-Loss On-Chip Transmission Lines and Inductors
G. Carchon, X. Sun, W. De Raedt, E. Beyne, IMEC-MCP/MaRS

Laser Trimmed Thin Film NiCr Embedded Resistor Tolerance
Sid Clouser, Jiangtao Wang, Rocky Hilburn, Gould Electronics

Ultra-Thin, Loaded Epoxy Materials for use as Embedded Capacitor Layers
Joel S. Peiffer, 3M Company

Comparison of HDI Organic and LTTC Substrate Technology with its Potential for RF Module Application
G. Sommer, Gerhard Fotheringham, W. John, H. Reichl, FhG-IZM

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Developments in Materials
Chair: Herbert Neuhaus, Scimaxx Solutions
2 pm - 4:35 pm
This session reports on the real-world application of some recent materials developments, including lead-free solder, adhesives for stacked die, and some new ceramic materials.

Development of Low-K Encapsulating Film for Stacked Packages
Akiko Matsumura, Kazuki Uwada, Yuji Hotta, Nitto Denko Corporation

Application of Spacer Filled Silicone Die Adhesive in Stacked Chip Technology
Xuan Li, R. Wayne Johnson, Auburn University; Thomas E. Noll, Michael J. Watson, Dow Corning Corporation

Synthesis of Ceramic Thin Films for Organic Board Compatible Integral Capacitors - Processing and Characterization
Devarajan Balaraman, P. Markondeya Raj, Isaac Robin Abothu, Swapan Bhattacharya, Michael D. Sacks, Rao Tummala, Georgia Institute of Technology; Michael J. Lance, Oak Ridge National Laboratory

Lead Free, Zero Shrink, Substrate Bonded LTCC System
R. L. Wahlers, A. H. Feingold, M. Heinz, Electro-Science Laboratories

The Investigation of Lead-Free Package Reliability
Jeffrey C. B. Lee, C. M. Chiang, Alejandro R. Cruz, Simon Li, Advanced Semiconductor Engineering

IMAPS Awards Ceremony
Tuesday, November 18, 2003
11:40 AM - 12:15 PM
Hynes Convention Center
ALL WELCOME!

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Technical Program

Tuesday, November 18, 2003

TP2
High Density Packaging
Chair: Rajen Chanchani, Sandia National Laboratories; Andrew Strandjord, IC Interconnect
2 pm - 5:25 pm

New technologies on ultra-thin, high density substrate, 3-D die-stacking and embedded passives will be presented in this session.

Three-D Vertically Stacked Electronic Structures for Array Sensors
R. Fillion, R. Wojnarowski, C. Kapusta, R. Saia, GE Global Research Center; K. Kwiatkowski, Los Alamos National Laboratory; J. Lyke, Air Force Research Laboratory

SIP Solution for High-End Multimedia Cellular Phone
Heung-Kyu Kwon, Tae-Je Cho, Se-Nyum Kim, Ki-Won Choi, Yun-Hyeok Im, Nam-Seog Kim, Heesook Lee, Dong-Kil Shin, Seung-Bae Lee, Jong-Bo Shim, Ki-Mيونg Yoon, Se-Yong Oh, Samsung Electronics Co., Ltd.

New Approaches to 3-D Interconnection Systems in Package Applications
Christian Val, 3DPlus

Ultra-Thin High-Density Packaging Substrate for High-Performance CSP and SiP
Tadanori Shimoto, Kazuhiro Baba, Hideya Murai, Wataru Urano, Hironori Ohta, NEC Corporation; Takehiko Maeda, Keiichiro Kata, NEC Electronics Corporation

Stencil Printing Technology for 100um Flip Chip Bumping
Dionysios Manessis, Rainer Patzelt, Technical University of Berlin; Andreas Ostmann, Rolf Aschenbrenner, Herbert Reichl, Fraunhofer Institute for Reliability and Microintegration (IZM)

Industrial Scale Manufacturing Process for Embedding Active Components Inside Organic Substrate
Petteri Palm, Risto Tuominen, Imbera Electronics Oy

Cross talk of Wiring in very Small 3D Module
Jarno Tanskanen, Eero O. Ristolainen, Tampere University of Technology; Janne Toikka, Aspiration Oy

TP3
Fine-Pitch Interconnection Technologies II
Chair: R. Wayne Johnson, Auburn University
2 pm - 5:25 pm

Recent advances in fine pitch interconnection technologies, both flip-chip and wire-bond, will be discussed in this session.

Flip Chip Bonding Technology for Molded Interconnect Device
Yoshihiko Yagi, Michiro Yoshino, Kojiro Nakamura, Kazuto Nishida, Manabu Kakino, Takayuki Hirose, Matsushita Electric Industrial Co., Ltd.; Fumikazu Harazono, Panasonic System Solutions Company

Filled No-Flow Underfilling - Process and Materials
Ning-Cheng Lee, Wusheng Yin, Hong-Sik Hwang, Indium Corporation of America

Very High Pin Count Flip Chip Assembly using Conductive Polymer Adhesives
James E. Clayton, Polymer Assembly Technology, Inc.

Novel Advanced Interconnects
Richard LaBennett, Salvatore Bonafe, Alan Huffman, Chad Statler, MCNC Research and Development Institute

Application of 35um Pitch Wire Bonding Technology to High Density Package
Yasuhide Ohno, Kazuto Ohmisha, Kunihiro Noguchi, Kumamoto University; Tsumori Takado, NEC Corporation

Bondability, Reliability and Yield Benchmarks for High Volume Specialty Gold Fine Bonding Wire
Heiner Lichtenberger, Michael Zasowski, Gery Lovitz, Williams Advanced Materials; Daniel Ha, YMC

Laser Direct-Write (LDW) Technology and its Applications in Low Temperature Co-fired Ceramic (LTCC) Electronics
David Liu, Chengping Zhang, John Graves, Todd Kegresse, Potomac Photonics, Inc.

TP4
Power Packaging Technologies
Chair: Douglas C. Hopkins, State University of New York at Buffalo
2 pm - 5:25 pm

New heat sink techniques start the session with one approach using nano-layered foils for 10X improvement. Unique device packaging approaches are next and include wafer level packaging of power FETs.

Multiscale Multiphysics Analysis of Wirebonds for Electronic Packaging
Ryszard J. Pyrputniewicz, Worcester Polytechnic Institute; Patrick W. Wilkerson, Andrzej J. Przekwas, CFD Research Corporation

Manufacturing and Evaluation of Thermal Expansion Behavior of Discontinuous Pitch Graphite Fiber Reinforced Copper Alloys for CTE Matching Heat Sink Applications
James A. Cornie, Shiyu Zhang, Metal Matrix Cast Composite, LLC

A Tenfold Reduction in Interface Thermal Resistance for Heat Sink Mounting
T. P. Weih, D. Van Heerden, O. M. Knio, Reactive NanoTechnologies

Thermal Performance and Microstructure of Lead-free Solder Die Attach Interface in Power Device Packages
D. Huff, D. Katsis, K. Stinson-Bagby, T. Thacker, G-Q Lu, J. Daan van Wyk, Virginia Polytechnic Institute and State University

New Generation Wafer-Level (Chip Scale) Package Technology Delivers Higher Levels of Power and Reliability Performance for Power MOSFET Devices
M. Kasem, E. Tjia, C. Chen, Vishay Siliconix

Development of SOIC Exposed Pad Package for Dual Die Power Products
Mervi Paulasto-Kröckel, Christina Bohm, Anton Kolbeck, Gary Johnson, Hubert Wieser, Motorola GmbH
Development of Silicon-Carbide (SiC) Static-Induction-Transistor (SIT) Based Half-Bridge Power Converters
A. B. Lostetter, S. Magan Lal, A. Mantooth, Aicha Elshabini, University of Arkansas; J. Hornberger, Arkansas Power Electronics International, Inc.; Kraig Olejniczak, Valparaiso University

TP5 Printed Wiring Boards
2 pm - 5:25 pm
The Printed Wiring Board Session is well balanced to cover a broad range of industry needs and new developments. Topics that will be covered include new processes, fine pitch manufacturing, new materials, design issues, thermal modeling, reliability evaluations, and systems applications.

Characteristics of Wet Etching of Copper Foil for Printed Circuit Boards by using Ferric Chloride Solution
Katsutoshi Matsumoto, Shoji Taniguchi, Tohoku University; Shingo Funahashi, Nippon Mining & Metals Co., Ltd.

Electrochemical Migration of Immersion Silver Finish: Test Vehicle and Material Evaluation
Jiming Zhou, Robert Clawson, Phil Wittmer, Rick Snyder, Jerry Badgett, Delphi Delco Electronics Systems

Evaluation of High Temperature Overmold Compounds for Manufacturing of Laminate Based Leadfree System in Package Mohammed Wasef, Mike Anderson, ANADIGICS, Inc.

New Manufacturing Process for Flexible Printed Circuit Board (PCB) with Cu Conductive Lines of 5 µm Pitch
H. J. Lee, Jin Yu, KAIST; T. Y. Lee, Hanbat University

Board Level Underfill for CSP Applications
Prakorn Vichulata, AMD Ltd.

Thermal Investigation for an Advanced Graphic Module Board
Eason Chen, Carol Liang, Jeng Yung Lai, Yu-Po Wang, C. S. Hsiao, Siliconware Precision Industries Co., Ltd.

Vertically High Density Interconnection for Mobile Application
Takayoshi Katahira, Ilkka Kartio, Nokia Mobile Phones; Hiroshi Segawa, Michimasa Takahashi, Katsumi Sagisaka, Ibiden Co., Ltd.

WAI MEMS Packaging
8 am - 11:25 am
As microelectromechanical systems (MEMS) become more widely used, new packaging challenges and opportunities continue to arise. This session covers state-of-the-art solutions in MEMS packaging for inertial, RF, and optical systems.

Vacuum Packaging of MEMS Inertial Sensors
Thomas F. Marinis, Joseph W. Soucy, Draper Laboratory

Novel Noninvasive Methodology for Characterization of Packaging for MEMS Inertial Sensors
Ryszard J. Przyputniewicz, Peter Hefii, Adam R. Klemppner, Cosme Furlong, Worcester Polytechnic Institute; Thomas F. Marinis, Joseph W. Soucy, Draper Laboratory

Low Cost Manufacturing/Packaging Process for MEMS Inertial Sensors

Low-Cost Packaging of Inertial MEMS Devices
L. E.Felton, M. Duffy, N. Hablutzel, P. W. Farrell, W. A. Webster, Analog Devices

Impact of Thermal Cycles During the Packaging Assembly Process on RF-MEMS Switch Performance
Ananda P. De Silva, Lianjun Liu, Henry G. Hughes, Motorola Semiconductor Products Sector

Low-Profile Packaging Solution for RF-MEMS Suitable for Mass Production
Frank Daeche, Günter Ehrler, Michael Weber, Andreas Meckes, Robert Aigner, Hans J. Timme, Infineon Technologies AG

Near Hermetic Air Cavity Plastic Packaging for Wireless, MEMS and Optical Applications
John W. Roman, Richard J. Ross, RJR Polymers, Incorporated

WA2 Novel Manufacturing Technology
Chairs: Christina Conway, Rockwell Collins, Inc.; Bob Palumbo, Kyocera America
8 am - 11 am
The pursuit of smaller, more functionalities and cheaper microelectronics demands low cost and robust manufacturing. This session highlights the latest developments in general manufacturing technologies, such as quality system implementation for fabless operations, manufacturing information exchange and PWB component placement optimization. This session also reports, from a manufacturing point of view, the progresses on laser wafer marking, low cost fine line thick film and LTCC.

Implementing a Quality System for a Manufactureless Semiconductor Company
Mary McDonald, Individual Solution Options/Quality Services, Inc.; Michael Madsen, SigmaTel Inc.

Improvement of Placement Accuracy by Placement Optimization
Timo Liukkonen, Nokia Corporation; Aulis Tuominen, Tampere University of Technology

Laser Wafer Marking at Die Level
Bo Gu, Rainer Schrann, Jack Gillespie, GSI Lumonics Inc.

Low Cost Fine Line Mo-Mn Thick Film for Microwave Applications
Ken Kuang, Lisa Hamel, Kevin Cotner, Jun Guinto, Kyocera America, Inc.

Manufacturability Study of LTCC Integrated Packages for High Performance, Low Cost RF SiP Modules
Matthew Hoppe, Greg Surbeck, Henry Moret, Kathy Green, Ditrans Corporation

An Investigation of the Properties of Newly Developed LTCC Materials for their use in Microwave Antenna
Shotaro Watanabe, Katsutoshi Nakayama, Kazunari Watanabe, Asahi Glass Co., Ltd.

Technical Program

WA3 
Reliability 
Chair: John Devaney, Hi-Rel Laboratories 
8 am - 11 am

This session consists of 7 papers each on a unique topic, 6 of which touch on an aspect of the reliability of components, substrates or materials used in the manufacture of various types of hybrids or multi chip assemblies. The seventh discusses a novel approach to failure analysis on complex circuits used in multi chip modules.

Effect of Hydrogen on GaAs MMICs in Hermetic Packages 
D. N. Goswami, Picosecond Pulse Labs

Effect of Isothermal Aging on the Intermetallic Compound Layer Growth in BGA Joints with Sn-Ag-Cu Solder 
Jeong-Won Yoon, Seung-Boo Jung, Sungkyunkwan University; Chang-Bae Lee, Samsung Electro-Mechanics Co., Ltd.; David J. Quesnel, University of Rochester

Contact Resistance of Anisotropic Conductive Adhesives 
Ranjith Divigalpitiya, 3M Canada Company; Peter Hogerton, 3M Company

A Comparison of Ion Diffusion and Moisture Diffusion in a Commercial Epoxy Molding Compound 
Leon Lantz, II, Michael G. Pecht, University of Maryland at College Park; Mark C. Wood, Army Research Lab.

The Significance of Glass Transition Temperature of Molding Compounds for Screening and Reliability Qualification of COTS PEMS 
Alexander Teverovsky, QSS Group, Inc.

Quantitative EDX the Effective Column Short Failure Analysis for High Density Integrated Circuit Devices 
Suntra Anuntapong, Nopphadol Kongtongnok, AMD Ltd.

WA4 
Thermal Management 
Chair: Ajay P. Malshe, University of Arkansas; Dave Saums, DS&A 
8 am - 11:25 am

The performance of thermal spreaders and heat sinks must keep pace with the demands of the electronic industry as “smaller-faster-lighter” is relentlessly pursued. More efficient and lighter weight thermal spreaders and heat sinks must continue to evolve through improvements in conventional technologies and/or the developments of new materials and technologies to ensure the efficient thermal management of electronic systems. In this session we have included a wide range of cutting edge topics addressed through modeling, experimentation and product development. We invite you to attend this important session, and we look forward for prolific discussions.

ALSiC for Optoelectronic Thermal Management and Packaging Designs 
Mark A. Occhionero, Richard W. Adams; Dave Saums, Ceramics Process Systems

Impact of Heat Spreading Lids on Flip Chip Thermal Performance; With and Without Heat Sink 
Jamil Wakil, IBM Corp.

LTCC Substrates with Internal Cooling Channel and Heat Exchangers 
Marc A. Zampino, Hari Adluru, Yanqing Liu, W. Kinzy Jones, Florida International University

Thermal Performance of a High End Flip-Chip Organic Package 
V. V. Calmidi, S. B. Sathe, Endicott Interconnect Technologies, Inc.

High Performance Dual Redundant (DR) Fan Modules - Installing a Diffuser Element to Optimize the Series Fan Configuration 
H. Harrison, HB Innovation Ltd.; F-S Lien, J. Jilesen, University of Waterloo

Development of a Process Friendly Film for High Performance Thermal Management Applications 
Andrew Collins, Chih-Min Cheng, Emerson and Cuming

Remote Heat Sink with Temperature Control using a Miniaturized Loop Heat Pipe 
Dimitry K. Khristalev, Thermacore International, Inc.

WA5 
Marketing Forum 
Chair: Michael P. O’Neill, Heraeus Inc. - CMD; Howard Imhof, Metalor Corp.; Adam Singer, Cookson Electronics 
8 am - 11:25 am

It is my great pleasure to welcome IMAPS 2003 attendees to the IMAPS Marketing Forum. The forum is FREE (yes, I said FREE) to all IMAPS 2003 attendees and is sponsored by the Microelectronics Marketing Research Council (MMRC). This forum has been designed to inform attendees of key market trends impacting several markets and technologies of interest to IMAPS attendees. These invited speakers are a dynamic group of industry experts. At the conclusion of the presentations, a panel discussion will look to challenge the speakers and the audience to discuss and debate their views on the current and future state of various segments of the microelectronics market.

Opening Remarks 
Michael O’Neill, Chairman, MMRC Steering Committee

Packaging is Leading the Recovery 
Jim Walker, Gartner Datasquest

Opportunities for Application Specific and Value Added Components 
Dennis Zogbi, Paumanok Group

Broadband Wireless Technology and Opportunities 
Jack Browne, Penton Media

Global Electronics Manufacturing - The China Wild Card 
Jan Vardaman, TechSearch International

The Wireless Industry - What’s Hot and What’s Not 
Don Brown, International Wireless Packaging Consortium

Panel Discussion 
Moderator - Jack Browne, Penton Media
**WP6**

Technology Drivers Trends for Electronic, Optical, Mechanical and Chemical Packaging Technologies toward Ubiquitous Network Age (Japanese Translated Session)


8 am - 11:25 am

New applications in Advanced Packaging Technologies, based especially on Nano, MEMS and sensing Technologies as part of the coming Ubiquitous Network Age. Recently developed examples such as modules, components, substrates and materials will be introduced.

Advanced Packaging Technology Trend for Mobile Terminals toward Ubiquitous Age in Japan

Tomiyo Ema, Panasonic Mobile Communications Co., Ltd.

A Battery-Less Wireless System using Ambient Heat with a Low-Voltage CMOS/SOI DC-DC Converter

Yoshifumi Yoshida, Fumiyasu Utsunomiya, Matsuo Kishi, Seiko Instruments Inc.; Norio Hama, Seiko Epson Corporation; Takakuni Douseki, NTT Microsystem Integration Laboratories

The Direct Methanol Fuel Cell (DMFC): Powering Portable Equipment in an Age of Ubiquitous Networks

Hirohisa Miyamoto, Toshiba Corporation

Micro Fuel Cells using Carbon Nanohorns: A Portable Power Source for a Ubiquitous Society

Yoshimi Kubo, NEC Corporation

The Status and Future of Optical Circuit Packaging Technology

Osamu Mikami, Tokai University

Robot Technologies for Human-Robot Cooperation Systems in Ubiquitous Age

Yasuhisa Hirata, Tohoku University

Ubiquitous Transducers for Health Care and Environmental Analysis

Kohji Mitsubayashi, Tokai University

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**WP1**

Sensors and MEMS

Chairs: David Galipeau, South Dakota State University; Richard Gehman, Honeywell Sensing and Control

2 pm - 5:25 pm

Sensor and MEMS applications continue to grow rapidly in traditional markets such as hazardous gas detection as well as newer areas like biomedical and RF MEMS. This session covers state-of-the-art sensors, systems, materials, and MEMS structures to measure hazardous gases, automotive emissions, and urinary pressure, as well as for RF applications.

Gasoline Vapor Sensor for Power Vent Water Heaters

Richard W. Gehman, Honeywell Sensing and Control

Screen-Printed Fe$_3$O$_4$/ZnO Thick Films for Gas Sensing Applications

K. Arshak, I. Gaïdan, L. Cavanagh, University of Limerick

The Application of Sensors in Automotive Emissions Testing

Delip “Doug” Bokil, Environmental Systems Products Holdings Inc.

Telemetry in Measuring Urinary Bladder Pressure

Bujjibabu Godavarthi, Joan Delalic, Michel A. Pontari, Michael R. Ruggieri, Temple University

Thermal Characterization of RF MEMS Relay Switch Design

Ryszard J. Pryputniewicz, Malgorzata S. Machate, Cosme Furlong, Worcester Polytechnic Institute; David Rosato, Harvard Thermal, Inc.

Design, Modeling and Simulation of Electrostatic Flexures for Microelectromechanical Systems (MEMS)

Muhammad Imran, William L. Ables Jr., University of Arkansas at Little Rock

Electroprohetic Photocressit for Patterning Three Dimensional Structures (How to make groovy patterns and not mind being in the pits)

Jill Steeper, Shipley Co., L.L.C.

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**WP2**

RF & Microwaves

Chairs: John Gipprich, Northrop Grumman Corporation; Fred Barlow, University of Arkansas

2 pm - 5:25 pm

Packaging and integration of RF & Microwave circuits is a growing and important area. This session includes presentations covering new packaging methods, material evaluation, and new materials tailored for these demanding applications. In addition, several speakers will discuss new filter designs and the integration of these designs into compact product form factors.

New Temperature Calibration Method for Digital Microwave Radio Transceivers

N. Hassaine, L. Villeneuve, F. Concilio, Harris Corporation

MCMs for Space Application: up to 40 GHz inside the Multilayer Ceramic

Claude Drevon, Chloë Schaffause, Jean-Louis Cazaux, Alcatel Space

Application of Uniplanar Structures for High Frequency Material Characterization

Can Eyup Akgun, Rhonda Franklin Drayton, University of Minnesota; Daniel I. Amey, Tim P. Mobley, DuPont Microcircuit Materials

Embedded Passives in Low-Temperature Co-Fired Ceramic for RF & Microwave Applications

M. Folk, V. Wang, A. Elshabini, F. Barlow, University of Arkansas

New LTCC Material with Zero TCF and Low Loss at 15GHz

Yoshiyo Umayahara, Masaru Iwao, Kazuyoshi Shindo, Nippon Electric Glass Co., Ltd.

Synthesis and Characterization of Particle Filled LTCC Tape for Wireless Communication Applications

Kyoung-Ho Lee, Sun-Young Kim, Soonchunhyang University

LTCC MLC Bandpass Filter using Quarter-Wavelength Hairpin Resonators for WLAN

Gyu-Je Sung, Hankyong National University; Dong-Hun Yeo, Korea First Microwave
technical program

Wednesday, November 19, 2003

WP3  Thick and Thin Film Material Processing  
Chairs: Michael Ehler, National Semiconductor LTCC Foundry; John Menaugh, DuPont Microcircuit Materials  
2 pm - 5 pm  
This session will highlight several new developments in ceramic substrates, especially LTCC, and new inks. Process topics include aqueous casting, fine line screen printing and a new thermal measurement method.

Lead and Cadmium Free Low Temperature Firing Thick Print Copper Inks  
Orville Brown, Srinivasan Sridharan, Ferro Corporation

New Approach to Thermal Conductivity of Thin Films Measurements by Means of Comparative Method  
Selim Achmatowicz, Iwona Wyzkievicz, Elzbieta Zwierkowska, Institute of Electronic Materials Technology; Wojciech Lobodzinski, Industrial Institute of Electronics

A Model of Fine Line Screen Printing on LTCC  
Shih Shao-Ju, Chiu Kuo-Chuang, Ricky Chen, Hung Ying-Chang, Lin Hong-Ching, Industrial Technology Research Institute

Dielectric and Magnetic LTCC Material System  

Comparative Study on Laser Trimming with Different Wavelengths  
Bo Gu, Bruce Couch, J.J. Oh, Paul Chase, GSI Lumonics Inc.

Development Thermoelectric Detectors on Base Higher Manganese Silicide (HMS) Films  
T. S. Kamilov, A. A. Uzokov, D. K. Kabilov, S. F. Ganib-taev, Tashkent State Aviation Institute; B. N. Zaveryukhin, R. A. Muminov, Physical Technical-Institute of the Academy of Sciences of Republic of Uzbekistan; V. V. Klechkovskaya, Shubnikov Institute of Crystallography

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WP4  Wafer Level Packaging  
Chairs: Michael Toepper, Fraunhofer IZM; Jamin Ling, ST Assembly and Testing Services (STATS - US)  
2 pm - 5:25 pm  
The importance of Wafer Level Packaging to a number of new and emerging technologies including traditional integrated circuit applications as well as MEMS and optoelectronic packaging applications is fueling the drive towards this form of packaging. This session will cover a host of applications involving wafer level packaging as well as some key developments in process technology which make these applications possible.

Bump Wafer Level Packaging - A New Packaging Platform (not only) for Memory Products  
Harry Hedler, Thorsten Meyer, Wolfgang Leiberg, Roland Irig, Infineon Technologies

New Wafer Level Structure for Stress Free Area Array Solder Attach  
R. Fillion, L. Meyer, K. Durocher, S. Rubinztajn, D. Shaddock, J. Wright, GE Global Research Center

Reliability of a Wafer Level Packaging method with Plastic-Core Solder Bumps: Utilizing Sn-Ag Solder at 0.3 mm Diameter  
Masto Sumikawa, Rina Murayama, Masashi Ogawa, Hiroshi Matsubara, Sharp Corporation

Room Temperature Bond for Wafer Level Packaging  
Helge W. Luessenbrink, Steven Dwyer, Markus Winplinger, Chad Brubaker, EV Group, Inc.; Paul Lindner, Thomas Glinser, Christine Thanner, EV Group GmbH

Wafer Level Vacuum Cavity Packaging for MEMS, Optoelectronics and Sensors  
George A. Riley, FlipChips Dot Com

Novel Method for Wafer-Scale Packaging of Opto-electronic Devices  
Daryl Spencer, Ajay P. Malhe, Ronald B. Foster, University of Arkansas; Chad B. O’Neal, SYSCON Corporation

Front End Compatible Wafer Level CSP-Technology for RF- and HT- Applications  
Klaus Burger, ATML Germany GmbH

WP5  Interactive Forum (Poster Session)  
1 pm - 4 pm  
EWOD Induced Fluid Flow for Biological Applications  
Ryan T. Marinis, Ryszard J. Pruputniewicz, Worcester Polytechnic Institute

Controlled Laser Ablation of Polymide Substrates  
Peter Gordon, Richard Berenyi, Balint Balogh, Budapest University of Technology and Economics

Epoxy Flux for Lead-Free Soldering  
Ning-Cheng Lee, Wusheng Yin, Indium Corporation of America

MEMS Sensors for Temperature, Pressure, and Relative Humidity Measurements  
Houri Johari, Ryszard J. Pruputniewicz, Worcester Polytechnic Institute

Modeling Fatigue Behavior of Electronically Conductive Filled Adhesive Joints under Cyclic Loading - A Novel Modeling Approach for Integrated Joint Life Prediction  
Rajesh R. Gomamat, Lehigh University; Erol Sancaktar, University of Akron

Reconfigurable Embedded Test for Improved System Reliability  
Kimberly E. Newman, University of Denver

Development of Au Reflection Film with High Adhesion for Optical Interconnection between LSI Chips  
Koichi Yokota, Ryohei Satoh, Yoshiharu Iwata, Kozo Fujimoto, Osaka University; Shogo Ura, Kyoto Institute of Technology; Kenji Kintaka, National Institute of Advanced Industrial Science and Technology

SnZnAl Lead-Free Solder with High Packaging Reliability  
Masayuki Kitajima, Tadaaki Shono, Fujitsu Limited; Satoshi Masuda, Fujitsu Laboratories

On-Chip Isolation in Wafer-Level Chip-Scale Packages: Substrate Thinning and Circuit Partitioning by Trenches  
S. M. Sinaga, A. Polyakov, M. Bartek, J. N. Burghart, Technical University of Delft
Thursday, November 20, 2003

THA1
Optoelectronics Packaging and Processes
Chairs: Shapna Pal, Department of Defense; Jeff Shakespeare, Consultant
8 am - 10:35 am

- Analytical and Experimental Characterization of an Optical MEMS Device
- Development of Optoelectronic Holography
- Tin-Silver Electroplating of Pb-free Wafer Bumps
- Hybrid Approach to Thermal Management of a FET Power Amplifier
- Flip Chip Technology for High Temperature Automotive Applications
- Cure Processing Effects of Conductive Adhesives as Solder Alternatives: Performance and Reliability
- Smith, Emerson & Cuming

- Techniques for Nondestructive Evaluation of MEMS at the Wafer Level
- Reference Furnace, Semiconductor Industry Association (SIA)
- Wanda O'Hara, Chih-Ming Cheng, Sherri L. Achen, I/O Assembly Systems

- Elimination of Epoxy Resin Bleed Through Thin Film Plasma Deposition
- Failure Modes of Flip Chip Solder Joints under High Electric Current Stressing
- Quantitative LGA/Substrate Assembly Contact Study from Pressure Sensitive Film Measurements
- Quantitative LGA/Substrate Assembly Contacts from Pressure Sensitive Film Measurements

- Mechanical Strength of Glass Ceramic Substrates in Land Grid Array Packages
- Flexible Thermal Management Circuits Bonded Directly to Aluminum Heat Sinks
- Effect of Die-Attach Adhesives on the Stress Evolution in MEMS Packaging
- Cure Processing Effects of Conductive Adhesives as Solder Alternatives: Performance and Reliability
- Smith, Emerson & Cuming

- Small Form Factor Fiber Optic Transceiver with Unique Design to Meet EMC/EMI/ESD and Thermal Requirements
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- Small Form Factor Fiber Optic Transceiver with Unique Design to Meet EMC/EMI/ESD and Thermal Requirements

- Mechanical Strength of Glass Ceramic Substrates in Land Grid Array Packages
- Mechanical Strength of Glass Ceramic Substrates in Land Grid Array Packages
- Mechanical Strength of Glass Ceramic Substrates in Land Grid Array Packages

- A Novel Planarization Process for Providing Global Planarity for IC Manufacturing
- A Novel Planarization Process for Providing Global Planarity for IC Manufacturing
- A Novel Planarization Process for Providing Global Planarity for IC Manufacturing

- Passive Component Integration in LTCC
- Passive Component Integration in LTCC
- Passive Component Integration in LTCC

- Estimation of Sn-3.0Ag-0.5Cu Solder Joint Reliability by Weibull Distribution and Modified Coffin-Manson Equation
- Estimation of Sn-3.0Ag-0.5Cu Solder Joint Reliability by Weibull Distribution and Modified Coffin-Manson Equation
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- Optoelectronics Packaging and Processes
- Optoelectronics Packaging and Processes
- Optoelectronics Packaging and Processes

technical program

The Effects of Solder Composition on Ball Fatigue Strength of Chip Scale Packages
Seun-gweon Ha, Flynn Carson, Y. C. Kim, G. S. Kim, ChipPAC Incorporated

Numerical Simulation of Underfill Cure Evolution in Chip-Scale-Package (CSP) Manufacturing Process
Rajesh R. Gomatam, John P. Coulter, Lehigh University

Nonepoxy-Based Underfill for CSP Assembly
Paul Morganelli, Rob Frimanson, Matthew Laffey, Douglas Katze, Emerson & Cuming Specialty Polymers

THA3 Emerging Technologies
8 am - 11:25 am

Papers in this session cover a wide spectrum of emerging packaging technologies including: nanomaterials, novel materials and assembly methods.

The Performance of Next Generation Semiconductor Molding Compounds for Array and Transfer-Molded Flip Chip Encapsulation
Louis Rector, Mark Dimke, Henkel Loctite Corporation

Electrical Properties of Ferrite-Dielectrics Multi-layer EMI Filters using Buffer Layer Moon Soo Park, Jae Hyuk Jang, Byeung Gyu Chang, Seung Gyo Jeong, Samsung Electronics

Mechanical Reinforcement for Sphere Attach Applications
Maureen Brown, Richard Jung, Jin Liu, John Stipp, Amir Fattahian, Sandy Shashipadme, Northrup Grumman - Kester

Novel Low-Cost Sol-Gel Derived Materials for Nano-Structured and Repairable Interconnects

THA4 Modeling and CAD
Chair: Luu Nguyen, National Semiconductor Corp.
8 am - 11:25 am

A good understanding of the performance and reliability of a new package will need established analytical as well as semi-empirical simulation tools. This session addresses the latest development in package thermo-mechanical analysis, hygro-thermo-mechanical prediction, together with high frequency electrical package simulation, and a view of the changing role of package design software.

Analytical Solutions of Thermal Stress Distribution in Plastic Encapsulated IC Packages
Zhongmin Xiao, Biao Wang, Nanyang Technological University

The Effect of Material and Dimension Related Parameters on the FIT-Figures of Interconnections in Reliability Calculations
Klas Andersson, Nokia Research Center; Olli Salmela, Jussi Särkkä, Markku Tammenmaa, Nokia Networks

Experimental Physics Based Structure Integrity Analysis for Reliability Prediction
Hua Lu, Ryerson University; Jesse Zhou, Rich Golek, Motorola

THA5 National Science Foundation & Sidney J. Stein Educational Foundation
Chairs: Leyla Conrad, Georgia Institute of Technology; W. Kinzy Jones, Florida International University

Reliability of Multilayer Capacitors as a Function of Furnace Conditions
Chris Williams, Alfred University

Fabrication of Microchannels in LTCC
Roxana Estevez, Florida International University

Organic and Inorganic Substrate Materials
Adam Brown, Arizona State University

Improving the Reliability of Active Metal Brazed Cu/AlN
Beth MacMichael, New York State College of Ceramics at Alfred University

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upcoming events

IMAPS Topical Workshop & Exhibition on
Optoelectronics Device Packaging

Radisson Hotel Bethlehem
Bethlehem, PA
October 7 - 10, 2003

Sponsored by:
International Microelectronics And Packaging Society (IMAPS)
and the Local IMAPS Keystone Chapter

General Chair: Raymond A. Pearson, Lehigh University
 rp02@lehigh.edu

Technical Chair: Ben Velsher, OptoVia Corporation
 velsher@optovia.com

Exhibits Chair: Elizabeth Stasik, NorCom Systems, Inc.
estasik@norcomsystemsinc.com

Building on the success of the last two year’s Advanced Technology Workshops (ATWs) on “Optoelectronics Packaging,” an expanded venue is planned for this year including an afternoon of vendor exhibits and Professional Development Courses (PDCs). This workshop will focus on recent advances in optoelectronics, packaging of optoelectronic devices and associated technologies. An outstanding program is planned with internationally recognized speakers from industry, academia and government.

Visit www.imaps.org/opto/ for more information

Advanced Technology Workshop on
High-Speed Interconnect, EMC and Power Aspects of
System Packaging for High Performance Computing
Telecom and Test Equipment

Sheraton Palo Alto Hotel
Palo Alto, California USA
October 19 - 22, 2003

Sponsored by:
International Microelectronics And Packaging Society (IMAPS)

General Chair:
Sarosh Patel, Teradyne Inc.
San Jose, CA USA
sarosh.patel@teradyne.com

Information will be posted on the IMAPS site as it becomes available:
www.imaps.org/systemspack/

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Advanced Technology Workshop on
Thermal Management for High-Performance Computing and Wireless Applications

Sheraton Palo Alto Hotel
Palo Alto, California USA
October 22 - 24, 2003

Sponsored by:
International Microelectronics And Packaging Society (IMAPS)

General Chair:
Dave Saums, Ceramics Processing Systems Corporation
Newburyport, MA USA
dsaums@msn.com

Information will be posted on the IMAPS site as it becomes available:
www.imaps.org/thermal/

IMAPS Advanced Technology Workshop on
Packaging Copper/Low-K Semiconductors

Red Lion Hanalei Hotel
San Diego, CA USA
December 15 - 17, 2003

Sponsored by:
International Microelectronics And Packaging Society (IMAPS)

General Chair: Andrew Strandjord, IC Interconnect
astrandjord@icinterconnect.com

Many benefits have been realized with the successful implementation of Copper metallurgy and Low-K dielectrics into the front-end manufacturing processes for semiconductors, including: increased device speed, reduced power consumption, denser circuitry, and reduced cost of manufacturing. This rapid shift from aluminum/oxide to Copper/Low-K semiconductors has also lead to the immediate need for new technologies in the back-end processes (packaging & assembly). The technical program for this ATW will focus on the latest packaging and assembly technologies for Copper/Low-K semiconductors.

Visit www.imaps.org/copper for more information
In conjunction with the IMAPS 2003 Symposium - Boston

IMAPS 5th Advanced Technology Workshop on Packaging of MEMS and Related Micro Integrated Nano Systems

Sheraton Boston Hotel
Boston, MA
November 20 - 21, 2003

Sponsored by:
International Microelectronics And Packaging Society (IMAPS)

General Chair: Ajay P. Malshe
University of Arkansas/HiDEC
Fayetteville, AR USA
Email: apm2@engr.uark.edu

For more information, visit www.imaps.org/mems/

Special Event at IMAPS ’03

Microelectronics Marketing Research Council (MMRC)

Presents a

MARKETING FORUM
WA5

Free of Charge for all IMAPS 2003 ATTENDEES!

The MMRC (Microelectronics Marketing Research Council) will offer a free-of-charge Marketing Forum to all IMAPS 2003 attendees who wish to participate. The Marketing Forum will be held on Wednesday morning, November 19, 2003, at the Hynes Convention Center, Boston, MA (Room number TBA).

2003 was forecasted as a year of continuing recovery for various segments of the microelectronics industry. This session will help clarify if those forecasts have been fulfilled, which technologies are “hot”, and which continue to struggle. With many companies resources stretched thin, how does this impact their ability to develop and deliver product? What was the impact of war, SARS, and the overall geopolitical environment on our industry? With manufacturing continuing its migration to low cost regions, how does this impact YOUR business? These questions and more will be addressed.

Speakers will discuss their analysis and insights into various current and emerging markets of interest to both current and prospective IMAPS members. Some of these markets are Passive Devices, WLAN, Automotive, Broadband, Wireless, manufacturing in China, etc. The Forum will feature five presentations (see page 26 for a list of topics) with a panel discussion at the end that will allow for audience participation in this not to be missed event!
Hotel Information

SHERATON BOSTON HOTEL**
Headquarters Hotel, Site of the IMAPS Welcome Reception
39 Dalton Street
Boston, MA 02199
Phone: 617-236-2000
Fax: 617-236-1702
Rates: **Single $199; Double $241; Club Level: $251**

You can also make your reservation on-line: Go to: www.starwood.com/sheraton/meetings/attend_enter_code.html.
In addition to making your room reservation, you can view a slide show of the hotel and general hotel information. You can also sign up for their award winning frequent guest program and Starwood Preferred Guest.
- Enter Boston, Massachusetts
- Meeting Code is 10850
- Select The Sheraton Boston Hotel
- Enter your Arrival and Departure Dates, Select Continue

Confirmation appears at the end and an email confirmation is also offered.

For reservations questions, email boston.sales@sheraton.com or call 800-325-3535.

HILTON BOSTON BACK BAY
40 Dalton Street
Boston, MA 02115
Phone: 617-236-1100 or 1-800-HILTONS
Fax: 617-867-6104
Rates: Single $200; Double $225; Triple: $249

Housing Deadline: October 3, 2003

Housing Accommodations MUST be made directly to the hotel of your choice. Please make your reservation before October 3, 2003.

A one night’s deposit is required to guarantee your accommodations.

All IMAPS room blocks will be released on October 3, 2003, after which IMAPS can not guarantee rates listed above.

**Headquarters Hotel.**

Three Convenient Ways to Register

On-line: www.imaps2003.org
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or

Mail this form to:
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For more information, please call IMAPS: 202-548-4001

Advance Registration
To register in advance for IMAPS 2003, your registration and payment information must be received no later than October 3, 2003. Register early and save $100. Register on-line at www.imaps2003.org and save an additional $50! All registrations received after October 3, 2003, will be considered “on-site registration.” Confirmations will be sent upon processing of registration form and payment. Those who register in advance may proceed on-site to Advance Registration to retrieve their badge and Proceedings at the Symposium.

Cancellation Policy
Cancellations will be refunded (less a $50 processing fee) only if written notice is postmarked on or before Friday, October 17, 2003. No refunds will be issued after that date.

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 Attendee Profile (Help IMAPS Provide a Better Service to You!)

1. What is your current primary job role for your company, organization or institution? As members often wear more than one hat, choose the category that best describes what subject occupies the largest percentage of your working time. [Check only one category, please, as the most relevant description. If you know that your role within your organization is changing in the near future to a new area, please select only that new area.]

   - Acoustics and airflow design
   - Advanced materials development
   - Basic sciences research and management
   - Circuit board layout and design
   - Circuit design for all types of analog and digital devices, except optoelectronic, RF, and power semiconductors
   - Circuit design for optoelectronic devices
   - Circuit design for RF devices
   - Circuit design for power semiconductor devices
   - Consultant
   - Corporate management
   - Education
   - EMC/EMI and all other forms of related emissions testing and system design for electronics of all types
   - Manufacturing engineering for all levels of component, modules, and systems assembly
   - Marketing and market research for electronics
   - MEMS/MOEMS component and system-related design
   - Optoelectronics device design
   - Packaging design for all types of analog and digital devices
   - Packaging design for module level devices, analog and digital
   - Packaging design for optoelectronic components and systems
   - Packaging design for RF components and systems
   - Packaging design for computing systems
   - Packaging design for telecom systems
   - Process engineering for materials and fluids used in electronics manufacturing
   - Purchasing
   - Quality control and quality assurance, including quality education for electronics of all types
   - Research and development focused on semiconductors
   - Retired
   - Sales
   - Semiconductor process design, manufacturing engineering, and manufacturing
   - Student – Graduate
   - Student – Undergraduate
   - Thermal management design for components, modules, and systems for electronics of all types

2. What is your primary educational background? [Check only one, please, as the most relevant description.]

   - Acoustics
   - Aerospace engineering and aeronautics
   - Business and industrial management
   - Ceramics
   - Chemistry
   - Chemical engineering
   - Civil engineering
   - Electrical engineering
   - Industrial engineering and industrial design
   - Marketing and marketing research
   - Materials sciences
   - Math and physics
   - Mechanical engineering
   - Metallurgy, mining, and metallurgical engineering
   - Optical and optoelectronics engineering
   - Quality control
   - Reliability engineering
   - Semiconductor and circuit design engineering
   - Other engineering
   - Other including liberal arts

3. How or at what general level do you contribute within your organization today? [Check only one, please, as the most relevant description.]

   - Consultant
   - Educator
   - Engineer
   - Manager – Engineering
   - Manager – Manufacturing
   - Manager – R&D
   - Manager – Other
   - Retired
   - Senior Executive Management
   - Student
   - Technician

4. What is the primary industry in which your division, subsidiary, or company sells the majority of the products that you are involved with? [Check only one, please, as the most relevant description.]

   - Automotive electronics and automotive electronics-actuated systems
   - Commercial semiconductor device manufacturing (not including military)
   - Computing systems
   - Medical electronics
   - Military and commercial avionics and other airborne electronic systems
   - Mil-grade and military semiconductor device manufacturing
   - Naval and commercial shipboard electronics
   - Optoelectronics and laser design and manufacturing
   - Power electronics systems for industrial applications
   - Power electronics systems primarily used in computing and telecom and related electronics systems
   - Space-borne electronics systems
   - Telecommunications systems
   - Test and measurement instrumentation
   - All or the majority of the above
   - Education (university and college level, consulting, educational services) to the electronics industry
   - Not Applicable – Student or Retired

5. What professional societies and organizations are you also a member of? [Check all that are relevant.]

   - ASME International
   - ACerS – American Ceramic Society
   - ACS – American Chemical Society
   - IEEE CPMT Society
   - IEEE MTTS Society
   - IEEE Other Society
   - IPC – Association Connecting Electronics Industries
   - MRS – Materials Research Society
   - OSA – Optical Society of America
   - SAE – Society of Automotive Engineers
   - SEMI – Semiconductor Equipment and Materials International
   - SMTA – Surface Mount Technology Association

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Family/Guest Information (if attending)

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Direct Mail  Advancing Microelectronics  Web  Email
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Total Fees and Deposits

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### Full Symposium Registration

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<tr>
<th>Type (check one)</th>
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<th>Advance (on/before 10/3)</th>
<th>On-site (after 10/3)</th>
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*Includes one-year membership or individual membership renewal at no additional charge.

### Professional Development Courses

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<td>Fundamentals of Fabrication &amp; Pkg....</td>
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<td>Overview of MEMS, MOEMS... CANCELLED</td>
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<td>New Development for Elect..(1/2 Day AM)</td>
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<td>Microsystems Packaging...(1/2 Day PM) Students Only - Free</td>
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<td>Advanced Packaging...(1/2 Day PM)</td>
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### Additional Events

- **Spouse/Guest Tours** WR, EX
  - 2 Day Package only $200
  - Tuesday & Wednesday $250
- **Golf Tournament**
  - $125 $150
- **Packaging of MEMS Workshop** - November 20 - 22, 2003
  - IMAPS Member $515
  - Non-member $615
  - Session Chair/Dealer $300

*Includes one-year membership in IMAPS.

### Foundation Contribution

- Sidney J. Stein Educational Foundation Contribution $_____

### Exhibit Purchase

- 10’x10’ Exhibit Space
  - $1800 members, $2300 non-members

- 10’x20’ Exhibit Space
  - $3600 members, $4100 non-members

No. of Booths ________ @ $________ Total $________
Company Name __________
Contact Name __________

### Additional Purchases

- Extra IMAPS 2003 Proceedings (Book or CD-ROM)
  - Book: $140 members, $215 non-members*
  - CD: $90 members, $165 non-members*

  (*Nonmember price includes 1 year IMAPS membership)

- Book Version Qty. ________ $_____
- CD-ROM Version Qty. ________ $_____

(All publications add $7 to ship in U.S.; overseas add $25)

### #3 Subtotal PDC Registration $_____

### #4 Subtotal Exhibit Sales $_____

### #5 Subtotal Additional Purchases $_____

### #1 Subtotal Symposium Registration $_____

### #2 Foundation Contribution $_____

### Early-Bird Discounts End October 3, 2003. Register Early • WWW.IMAPS2003.ORG
Exhibit Hall Aisle Signs

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Boston is known as one of the most historical, cultural and intellectual centers of our country. Boston, more than any other American city, is where our nation’s history began. There are many points of historical interest to visit while in Boston and most can be explored by foot – giving Boston its name “America’s Walking City.” Some of the names carrying a patriotic ring include Boston Common, The Freedom Trail, Boston Harbor, Beacon Hill and the famous Fanueil Hall Marketplace. Boston’s North End is a treasure trove of significant Revolutionary War sites. Ben Franklin and Paul Revere were both prominent North Enders. Still standing in the North End are Paul Revere’s home and the famous Old North Church whose tower lit the silent message “one if by land and two if by sea.”

If the days full of symposium activities and Boston’s local sights haven’t tired you enough, there’s plenty of nightlife. You can just sit back and enjoy the street entertainment and people watch at the famous Fanueil Hall and Quincy Marketplace or enjoy the fun at one of the neighborhood pubs. There’s a large variety of jazz clubs and discos to choose from, too. Conveniently connected to the Hynes Convention Center is “The City Under Glass.” Here you’ll find an amazing array of shops and an exciting variety of food at some of Boston’s most impressive restaurants. All in the heart of Boston’s fashionable Back Bay. Visit the Shops at Prudential Center at 800 Boylston Street and experience our city under glass.

You will experience the beginning of a spectacular New England fall when the daytime warm temperatures slip to crisp autumn nights. Follow the Freedom Trail and tread on the same cobblestones that John Hancock, Ben Franklin, John and Sam Adams and Paul Revere once walked over two centuries ago. Visit the decks of the USS Constitution or visit the gas lit Newbury Street chic boutiques and cafes just one block away from the Hynes Convention Center and Copley Square. From the great scrod and lobster to the wonderful Italian cuisine of the charming “North End” to the quaint Irish pubs, there is an endless choice of local selections to keep your appetite satisfied for a lifetime.

Boston

America’s Walking City

For Visitor Information, Call Toll Free

1-888-SEE BOSTON

http://www.bostonusa.com/

For Boston’s Back Bay area map (Hynes Convention Center and the Copley Square area hotels):

http://www.mccahome.com/Directions/images/map.gif

For a full Boston and Cambridge map:

http://www.mccahome.com/Directions/images/map2.gif

Other related and informational Links:

http://www.bigdig.com/

http://www.mbta.com/
The 37th International Symposium on Microelectronics will be held at the Long Beach Convention Center, Long Beach, CA. It is sponsored by the International Microelectronics And Packaging Society (IMAPS). The IMAPS Technical Committee seeks original papers that demonstrate how new technologies and applications are expanding and redefining the international role of microelectronics. All abstracts submitted must represent original, previously unpublished work.

**General Chair: Maurice Lowery**  
Northrop Grumman, maurice.lowery@ngc.com

**Technical Program Chair: Michael Ehlert**  
National Semiconductor LTCC Foundry, mikeehlert@cox.net

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### Papers are being sought from, but not limited to, the following subjects:

- Advanced Materials & Processes
- Advanced Substrate Technology
- Area Array Assembly
- Automotive Electronics
- Chip-Scale Packaging/Flip Chip
- High Density Displays
- High Density Packaging
- Low Cost Packaging Methods
- Management & Marketing
- Manufacturing Technologies
- Medical Electronics
- MEMS Packaging and Applications
- Modeling & Simulation
- Novel Interconnections
- Optoelectronics/Photonics
- Polymer Materials & Applications
- Power Packaging/Thermal Management
- Printed Wiring and Flex Boards
- Quality & Reliability
- RF/Microwave — Wireless
- Sensor Packaging & Applications
- Space & Military Electronics
- Statistical Process Control Methods
- Surface Mount Technology
- System Level Packaging
- Thick & Thin Film Materials

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**Cash Awards Offered**  
To reward exceptional work, IMAPS offers awards based on technical content, originality and applicability to current issues. Awards are presented in the following areas:

**Best Paper of the Symposium Award**  
**Cash Award**  
IMAPS offers a cash award of $2000 for Best Paper of the Symposium. The IMAPS Technical Committee chooses the Best Paper based upon evaluations submitted by the members of the Technical Subcommittees and the Symposium Session Chairs.

**Outstanding Paper Award**  
**Cash Award**  
IMAPS offers a cash award of $500 each for two (2) papers designated as Outstanding Papers of the Symposium. The IMAPS Technical Committee selects the two (2) Outstanding Papers based upon evaluations submitted by the members of the Technical Subcommittees and the Symposium Session Chairs.

**Best Paper of Session**  
These awards are based on technical quality and originality of written manuscripts. Only the Top 5 Best of Session papers are considered for Best Paper of the Symposium and Outstanding Paper awards.

Please send your 250-300 word abstract **electronically only** by March 12, 2004, using the on-line submittal form at: www.imaps.org/abstracts.htm

**Abstract Cut-off Date:** March 12, 2004  
**Notice of Acceptance:** April 16, 2004  
**Final Manuscripts Due:** July 30, 2004

If you are having problems with the on-line submittal form, please email Jackki Morris-Joyner jmorris@imaps.org or call 305-382-8433.

**See You Next Year in Long Beach, California • November 14 - 18, 2004**
<table>
<thead>
<tr>
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**MEMS ATW**
Sheraton Boston Hotel
November 20 - 21, 2003
For more information, visit: www.imaps.org/mems or see page 34.
You can also register on page 38.

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