SEMICONDUCTOR PACKAGING TRENDS

WHY THE FUTURE MUST BE DIFFERENT THAN THE PAST

Feature Size

Feature Size

350
300
250
200
150
100
50
0

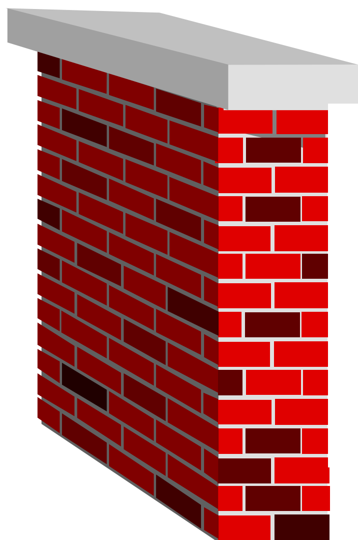
1996 1998 2000 2002 2004 2006

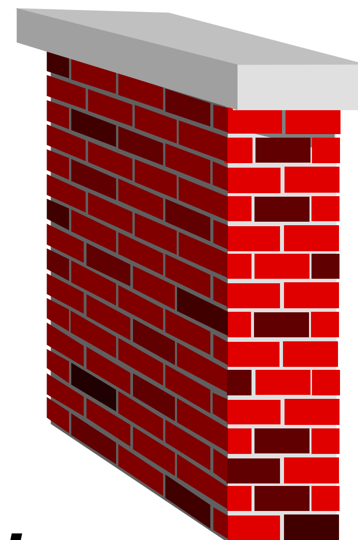
Copper Interconnects

Low K Dielectrics

The Good Old Days

Throw It Over The Wall





FAB

Assembly

PCB Assembly

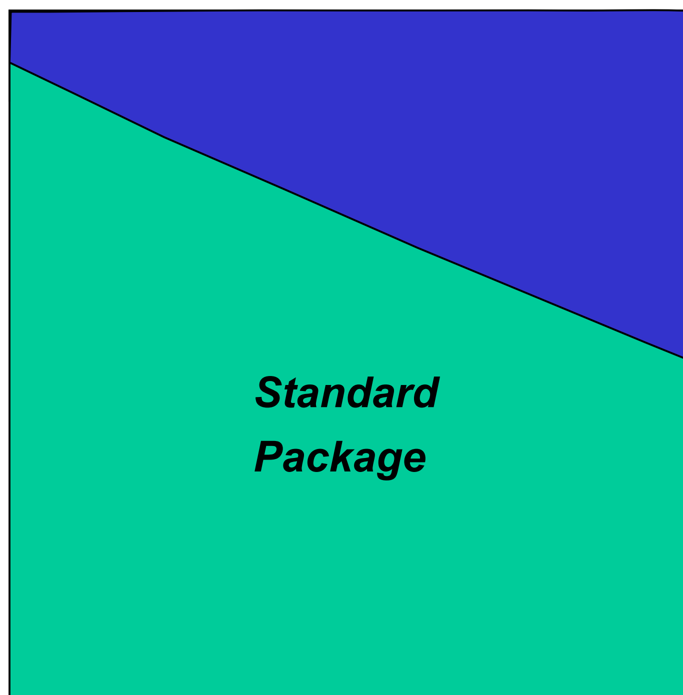
The Challenge

If we just linearly extrapolate our current industry organization and culture, the industry won’t successfully exploit coming advances in wafer fab technology.

The Shift to Application Specfic Packages

% OF ALL

PACKAGES



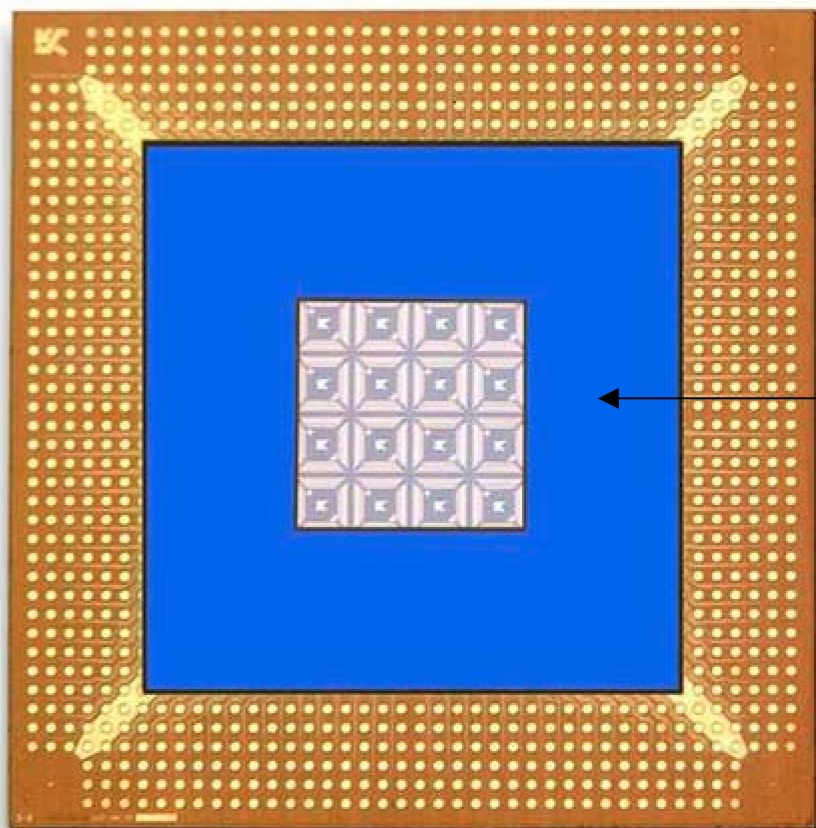
Application
Specific
Package

TIME

Why Package Chips?

- Physically protect chip
- Thermal management
- Provide electrical connection to the chip - “space transformation”
- Sometimes provide additional routing layers

Space Transformation



Package acts as space transformer to bridge tight pad spacing of chip and coarse spacing of PC Board

Reduced Feature Size Drives Space Transformation Requirement

Reduced Feature Size → More Transistors with constant chip size → Constant I/O Count Memory

More Transistors with constant chip size → More I/O's (ASIC, DSP, etc.) → Increase I/O Density

Reduced Feature Size → Reduced Chip size Constant Transistor Count (Standard Logic) → Increase I/O Density

Increase I/O Density → Greater Space Transformation Required

Space Transformation Trends

I/O density increases rapidly while PC board trace density is relatively static, so space transformation needs increase over time

Pad Pitch vs. Feature Size

Pad Pitch (microns)

120
100
80
60
40
20
0

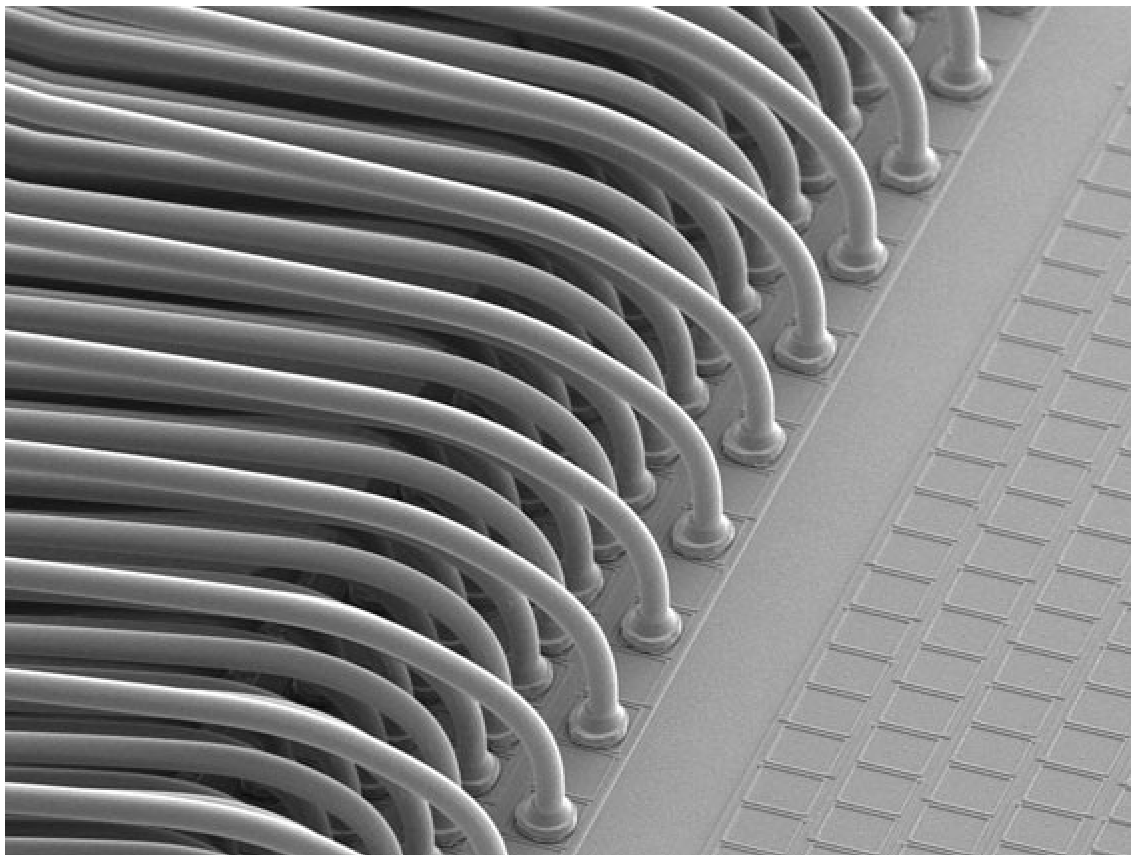
Linear scaling of pad pitch with feature size

What actually happened

300 250 180 150 130 70

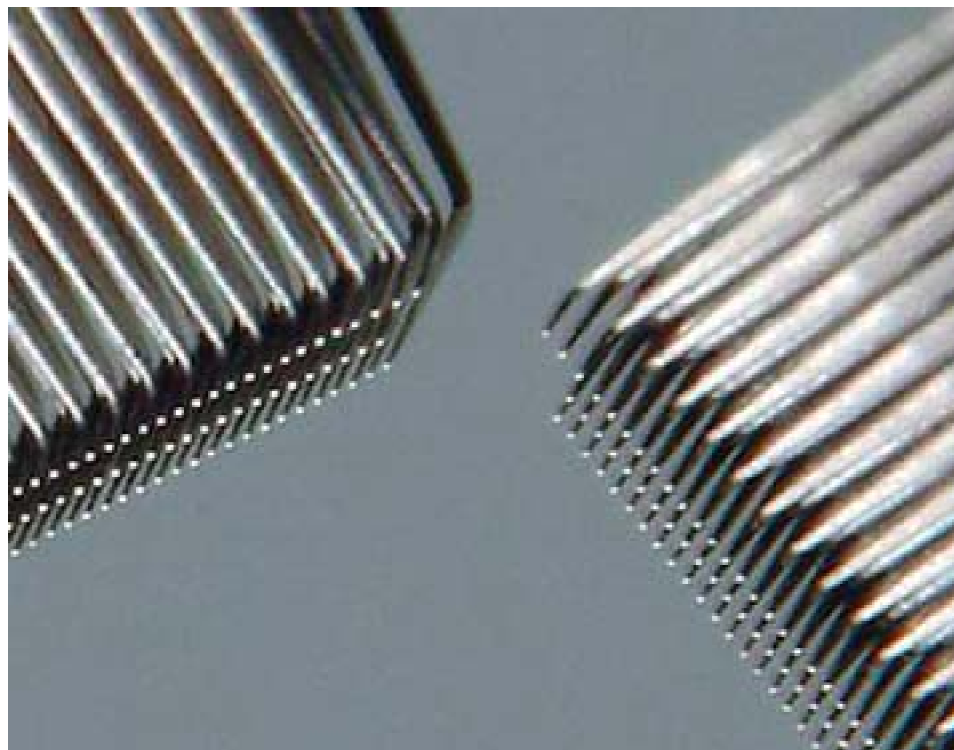
Feature Size (nm)

Multiple Rows of Bond Pads

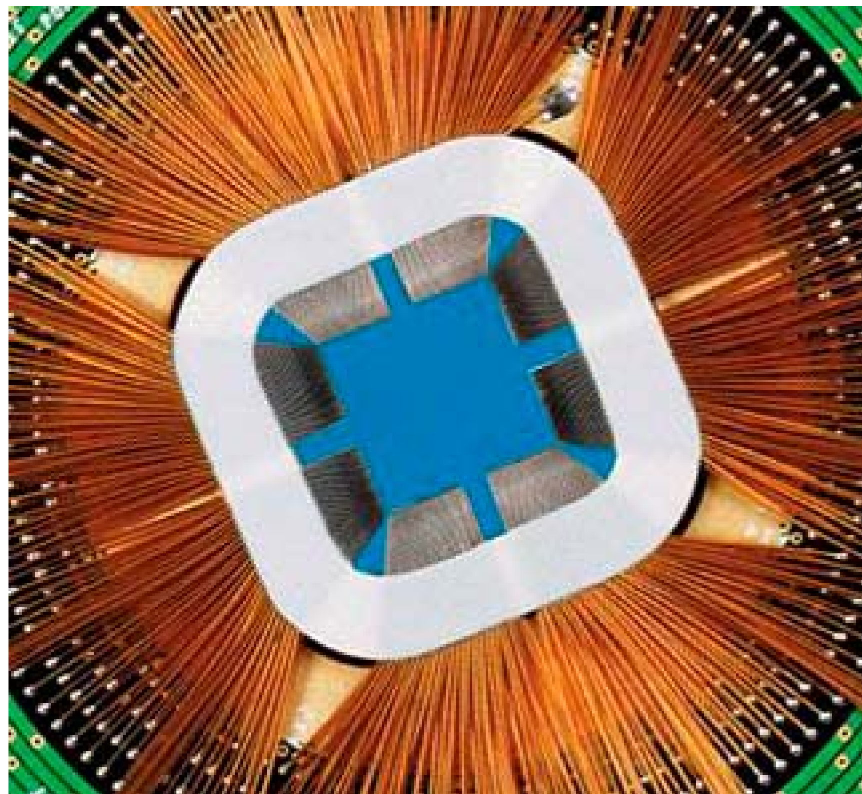


Very High Density Wire Bonding

Cantilever Probe Card for Multiple Rows of Bond Pads



High Density Cantilever Probe Card

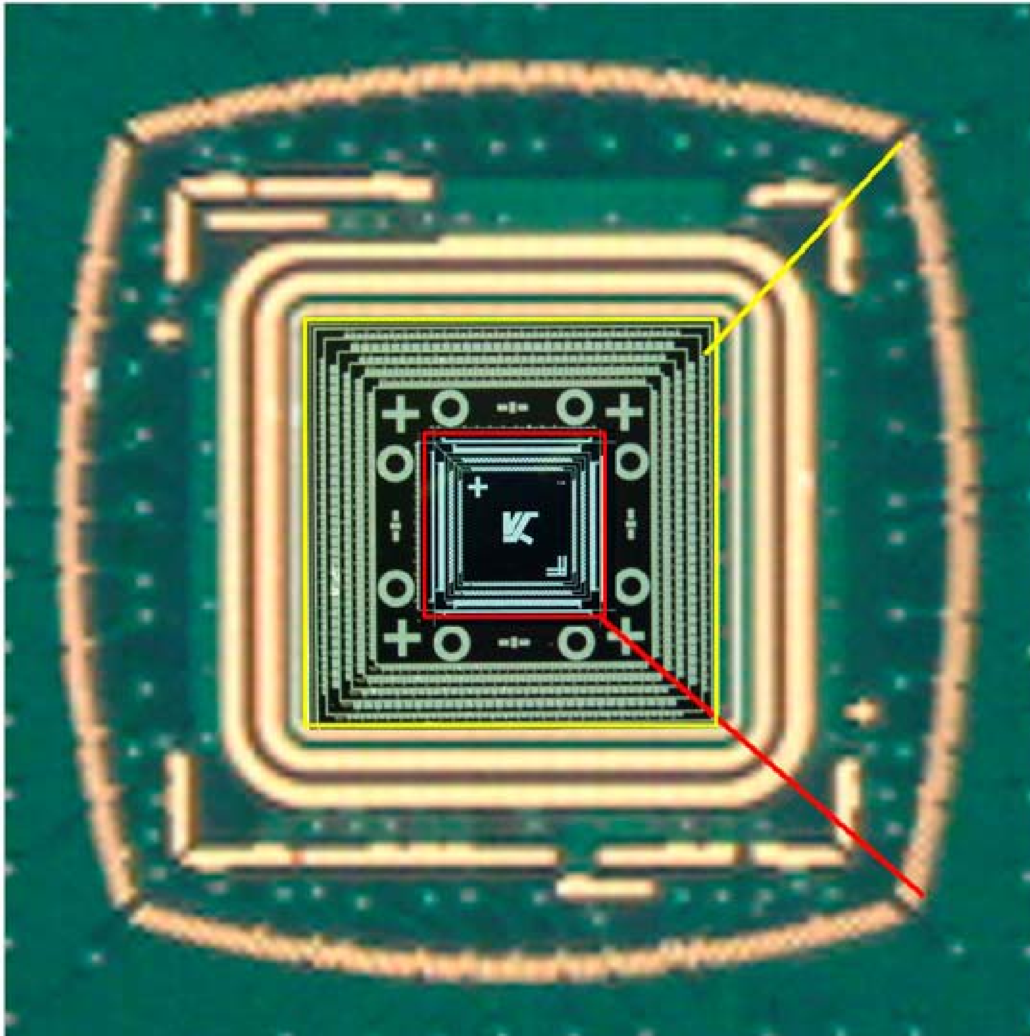


The Wire Sweep Challenge

Baseline Startposition (x = 564; y = 159)
Baseline Endposition (x = 132; y = 471)
Perpendicular point (x = 131; y = 468)
Baseline = 532.886
Distance to Baseline = 2.82843
Wiresweep Percentage = 0.530775%

12/04/2000
12:41:25
S/N 1 East 1

Pad Pitch vs. Wire Length



Die Shrink Effect On Wire Lengths 70 vs. 35µm In-Line Pitch

- 376 Die pads (80% signal, 20% power / ground) for illustration purposes
- 50% Reduction in die size (267 vs. 134 mils)
- 33% Increase in wire lengths (5.0 vs. 7.5mm)
- 60% Reduction in wire diameter (25 vs. 15µm), impacting wire sweep due to molding process

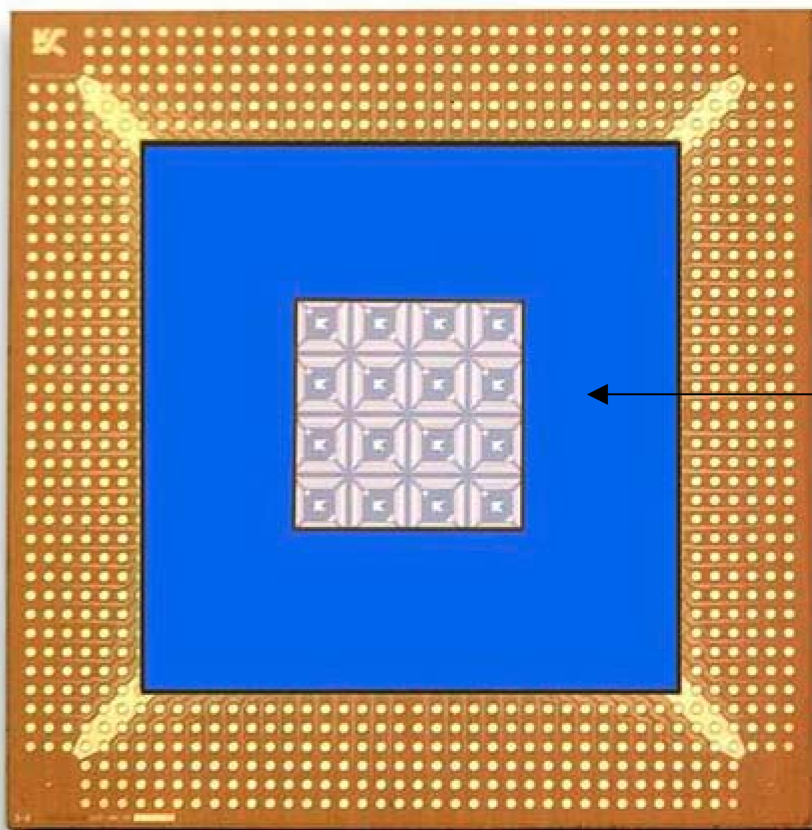
Very Long Wire Bonds

Fine Line Substrates Allow Short Fine Pitch Wire Bonds

High Density Wire Bonding
Multiple Rows of Second Bonds

No Sweep™ Stabilized Wire Bonds Using Liquid Encapsulate Prior to Molding

Space Transformation



Package acts as space transformer to bridge tight pad spacing of chip and coarse spacing of PC Board

Space Transformation

	LOW	HIGH
HIGH	DSP'S	Asic's Microprocessors
LOW	Standard Logic Analog Discrete	MEMORY

I/O COUNT (vertical axis)

TRANSISTOR COUNT (horizontal axis)

Space Transformation Drives Packaging Technology

2002

FLIP CHIP

HIGH

Asic's

Microprocessors

I/O COUNT

WIRE BOND

Standard Logic

LOW

Analog

Discrete

WAFER LEVEL PACKAGING

LOW

HIGH

TRANSISTOR COUNT

- *Large majority of all parts wire bonds*
- *Wafer level processing gaining initial acceptance for low I/O parts*

Typical Wafer Level Package Architecture

Al Pad

1st Passivation Layer

SiN Passivation

Wafer

UBM &
RDL Layer

2nd Passivation Layer

No additional passivation in
the streets

Solder Ball

- 1st Passivation — Planarization / dielectric
- UBM — Al/NiV/Cu Redistribution traces and Under bump metal
- 2nd Passivation — Final passivation to protect runners / defines solderable area

Space Transformation Requirements Drives Package Technology

Future Trend

- *Flip Chip space continues to expand*
- *Flip Chip space segmented between wafer level bumps and stud bumping*
- *Memory adopts wafer level package*

Wire Bonding Can Support High Switching Speeds

Wirebond vs Flip Chip: 2004 -2010 %

Wirebond vs Flip Chip Interconnects

Chart labels	
Y-axis	Billions of Leads %
Y values	0%, 20%, 40%, 60%, 80%, 100%
X values	2004, 2005, 2006, 2007, 2008, 2009, 2010
Legend	Wirebonded Lead Count; Flip Chip Lead Count

VLSI Research 7/05

Flip Chip Transition Challenges

- Redesign chip for area array vs. redistribution
- Vertical probe
- Bump metallurgy and fabrication process
- Multilayer substrates
- New assembly processes
- Qualify reliability of the flip chip system

Typical Vertical Probe

Probe head contacting ball array with 3,500 probes

Flip Chip Transition Challenges

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- Qualify reliability of the flip chip system

Array Pitch vs. Feature Size

Linear scaling of array pitch with feature size

Array Pitch (microns)

300
250
200
150
100
50
0

250 180 150 130 100 70

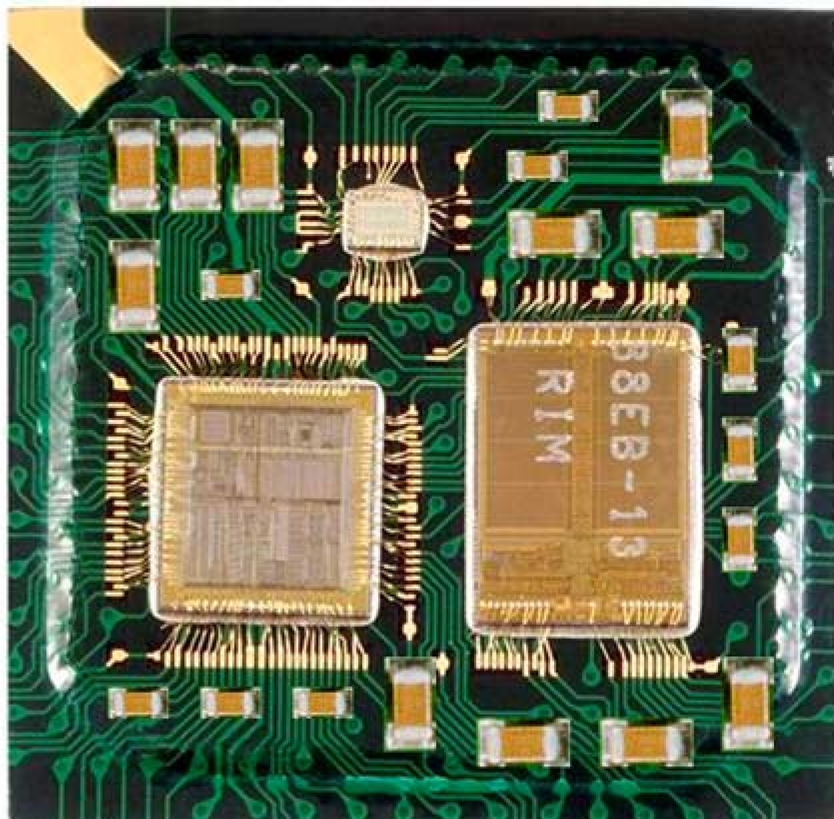
Feature Size (nm)

Mechanically Applied "Stud Bump"

Package as Part of Signal Routing in Microprocessor

Wafer
Silicon Substrate
Millions of Transistors on Substrate
Wafer Interconnect Levels
Top Metal Layer
Thousands of Wafer Bumps
Package Interconnect Levels
Package Substrate
From Package To Mother Board
Hundreds of Solder Spheres
PC Board

System In A Package



Stacked Die

Space Transformation Requirements Drives Package Technology

Future Trend

HIGH

Asic's
Microprocessors

FLIP CHIP

I/O COUNT

Standard
Logic

Analog

LOW

Discrete

WAFER LEVEL PACKAGING

LOW

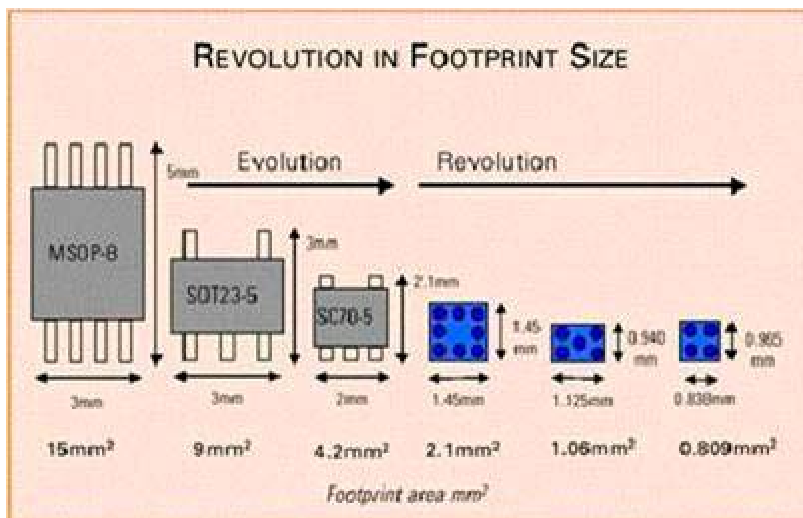
HIGH

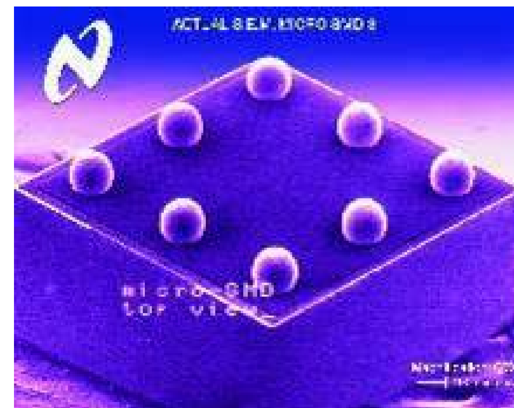
TRANSISTOR COUNT

- ***Flip Chip space continues to expand***
- ***Flip Chip space segmented between wafer level bumps and stud bumping***
- ***Memory adopts wafer level package***

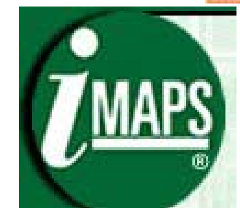
Wafer Level Package

- Low Pin Count Application
  - Temperature sensors, regulators (voltage, dropout, etc.) operational amplifiers, power amplifiers
    - 4, 5, and 8 I/O devices





Source: National Semiconductor



Wafer Level Package

Wafer Level Packaged Memory

Convergence

Wafer Fab

I/C Assembly

PC Board Assembly

Virtual Integration

FAB

ASSEMBLY

BD ASSEMBLY

Copper
Low K
Barrier Layers
Bumps
Wafer Level Packages
Testability
I/O Density
Signal Integrity

I/O Density
Signal Integrity
Testability
Thermal Management

System Level Design Tools
System in a Package

Virtual Integration Starts With Communication