A Modeling Method For The Study Of Thermomechanical Behavior Of High Density Interconnect (HDI) Vias

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Abstract

The thermomechanical behavior of High-Density Interconnect (HDI) vias has been numerically modeled taking into consideration the process-induced residual stresses. In this work, a two-step global-local scheme is implemented. The global model enables the computation of displacements, while the local model enables the computation of strains and stresses in the fine via structures. As the dimensions of the via structures are several orders of magnitude smaller than the dimensions of the HDI structure, a global-local modeling scheme is necessary for computational efficiency without losing accuracy. The models developed in this work can be utilized up-front in the design stage to select material, geometry, and processing parameters prior to undertaking extensive prototyping and reliability testing. Results from the global model used as input to the local model are validated using laminated plate theory analysis. Preliminary predictions of thermal fatigue failure of vias are also provided and are compared to experimental data.

Key words:
High Density Interconnect, Vias, Thermomechanical Modeling, Reliability, Warpage, and Via Fatigue.

1. Introduction

The electronics industry continues to expand the functionality and performance of electronic devices by increasing the integration levels of the chips. The increased chip-level integration has spawned new methods of packaging the chip to handle the expanding number of I/Os. The shift from traditional through-hole packages in the mid-1980s was accentuated by the displacement of the dual-in-line package (DIP) in select applications by surface mount technologies (SMT) such as quad flat packages (QFP) and area array packages like ball grid arrays (BGA). Recently, selected SMT applications are being displaced by a combination of chip-on-board (COB) and multichip module (MCM) technologies.1

One of the major issues that has arisen is the availability of materials for printed wiring board (PWB) substrates that are compatible with product and process needs. Furthermore, the increasing complexity of interconnect structures are pushing the limits of PWB technologies. To be able to keep pace with the large scale IC integration, High Density Interconnect (HDI) solutions are being increasingly pursued. Figure 1 shows a typical high density interconnect structure on a substrate. The HDI is a system of alternating layers of conducting and dielectric materials. Communication between conducting layers across the dielectric is accomplished through vias. The rapid growth in HDI technology has put severe demands on packaging in terms of increased wiring and via structure densities without increasing the signal delays, and simultaneous switching noise, among other factors. Typically, the vias encountered in multilevel thin film structures may be broadly classified into (i) planar, filled or studs (stacked), and (ii) non-planar, un-filled vias (spiral or staircase)2, as shown in Figure 2.

Although HDI offers design flexibility and wirability, the thermomechanical reliability of the HDI structures poses a concern,
mainly since these structures are susceptible to excessive warpage in large-area processing, interfacial delamination, and/or via cracking under processing temperatures and extreme in-service conditions. Traditional industrial practice to qualify microelectronic packages involves building prototypes and subjecting the prototypes to extensive reliability testing. The dimensions and materials used in producing these prototypes are often based on past experience. Facing the situation of new materials, new processes, and new designs, there is often no “past experience” to guide, and the initial few prototypes could lead to misleading results, if not carefully designed and fabricated. As the experimental prototyping and testing process takes several weeks to complete, every time a wrong design choice is made, time and cost present a great loss in the qualification process. The objective of the current work is to develop a comprehensive numerical model which can predict, up-front in the design phase, various thermomechanical reliability problems with HDI structures and aid in the selection of suitable materials, geometric parameters, and processing conditions prior to prototype fabrication and testing.

Among the various modeling studies, Akhavain and McCarty used an axisymmetric, single time-step, linear analysis with a temperature change of 1200 °C to study the tungsten vias in a ceramic multilayer structure. The thermal loading was indicative of the cool-down from densification at sintering. In this work, the ceramic was modeled with materials possessing linear elements, and tungsten was modeled with materially nonlinear elements. Figure 3 illustrates the configurations modeled in their work. Based on their study that included single via, staggered via, and stacked via configurations, the authors concluded that the stacked vias exhibit the maximum magnitude of stress compared to the single or the staggered vias. In addition, the researchers found that the effect of a given via on neighboring vias was negligible, provided that the via is at least one via diameter away from the edge of the neighboring vias. Using a theoretical model developed at Unisys, Akhavain and McCarty also calculated the tangential stress for a single via as a function of via radius and the distance from the center of the via and showed that the analytical and Finite Element results were very closely matched.

Analysis of the General Electric Chips-First Module constitutes a major portion of efforts in the thermomechanical reliability of HDI structures with vias. The Chips-First module is a copper/polymer HDI structure where the chips are placed in wells in a ceramic substrate followed by the application of the HDI layers onto the substrate, as shown schematically in Figure 4. The study by Prabhu et al., to determine the fatigue life of the HDI layers on the Chips-First module employed a 2D plane-strain Finite Element model and showed that the effect of introducing of a fillet in the corner of the via/via pad interface on the fatigue life was negligible. Another work by Wu et al. studied the residual stresses resulting from the HDI build-up process using 2D plane-strain and 3D Finite Element models. It was found that the residual stresses resulting from processing could exceed the yield stress of copper, and thus neglecting these stresses could result in erroneous reliability predictions. Comparison of the numerical predictions from DiTomasso’s study of the Chips-First module using plane-stress, plane-strain, axisymmetric, and 3D Finite Element models to experimental results obtained by Read et al. revealed that the most significant factors impacting via wall strain are the via wall thickness, the via wall angle, the top pad thickness, and the dielectric material.

Figure 1. Schematic of a HDI structure with a close-up view of a via.

Figure 2. Via structure types: spiral, stud, and stair-step.

2. Previous Thermomechanical Modeling of HDI Vias

The HDI structure with vias is a relatively new technology, and hence limited literature exists on the modeling of these structures.
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In summary, analytical formulations developed thus far have not accounted for the complex details of via geometries as well as the anisotropic, time- and temperature-dependent behavior of the materials used in multilayered structures. On the other hand, the numerical studies have not addressed some key issues. For example, studies by Prabhu et al. and DiTomasso assume that the stress-free temperature of the HDI structure is the room temperature and thus neglect the important residual stresses incurred during processing. As stated by Wu et al., this is a major source for error in reliability predictions. Furthermore, most of these studies are limited to the Chips-First module. Finally, no rigorous and systematic study has been conducted on the effect of material, geometry, and processing parameters on via reliability.

3. Objectives and Scope of the Research

The objective of this paper is to present a modeling methodology to understand the thermomechanical behavior of HDI via structures taking into consideration the process-induced stresses using a frozen-view modeling approach. The in-plane dimensions of the HDI structure are typically about five orders of magnitude larger than the via dimensions. Therefore, a Finite Element mesh fine enough to capture the local stresses within the vias may be too large from a computational perspective. On the other hand, a coarse mesh that can satisfactorily capture the global behavior may be inadequate to accurately determine the stress/strain distribution within the vias. In light of this fact, a two-step global-local approach has been implemented in this work. The global-local modeling approach presented in this paper will facilitate a systematic study of the effect of several geometry, material, and process parameters on the via reliability. For results from such a parametric study and for detailed dimension, material property, and process parameter variations, readers are referred to Reference. In addition to outlining the modeling methodology, this paper also presents warpage and via fatigue life predictions with comparison to closed-form analysis results and experimental data.

4. Global Geometric Modeling

Two types of models were created to determine the global deformation in a single-sided HDI structure. In the first type of global model, as shown in Figure 5, alternating layers of metallization and dielectric were represented as homogeneous layers with at least two rows of elements per layer. This global model did not include any intricate via shape. In the second type of global model, the interconnect vias were approximated by staggering element material properties to resemble a spiral via pattern as shown in Figure 6. In both types, only the right half of the geometry was modeled making use of the symmetry about the y-axis, as represented in Figures 5 and 6. It should be pointed out that, although the staggered-element model (Figure 6) was a closer representation of the actual HDI structure, this detailed model contained over 12 times the number of elements contained in the homogeneous-layer model (Figure 5). Due to this fact, the computation times for the staggered-element model were typically greater than the computation times for the homogeneous-layer model by a factor of about 24.

Figure 4. Schematic of the General Electric Chips-First HDI module.

Figure 5. Schematic of a single-sided global model without vias (not to scale).

Figure 6. Schematic of a single-sided global 2-D model with staggered vias included (not to scale).
upper layers due to the presence of the vias, which in turn, reduces the overall CTE mismatch between the base-layer and the HDI layers. Also, the predicted warpage is less for the 2x-pitch structure compared to the 4x-pitch structure due to the presence of more copper in the 2x-pitch structure. When the simulations were repeated for other base-layer thicknesses and other base-layer materials, it was found that, in general, the error in warpage prediction was less than 6%, if one were to not account for the via structure in the global model. As the via-free homogeneous-layer models have a higher warpage compared to staggered-element model, the results from the via-free global models are conservative. In addition, the models without vias require less computational time. For these reasons, the global models without vias were constructed to obtain the cut-boundary displacements to be applied to the local models.

5. Local Geometric Modeling

The local model is essentially a cut-section out of the global model, as shown in Figure 9, that includes the detailed geometry of the via structures. The cut-boundaries of the local model were extended by a distance that is half the via pitch from the centers of the first and the last via.

![Figure 9. Cut boundaries of local model for extraction from global model (not to scale).](image1)

Each local model contained six vias as illustrated in Figure 10. The three staggered vias located in the middle were used to study the effects of geometry, material, and processing parameters on via stresses and strains. It is pointed out that the present study primarily focused on spiral via configuration.

![Figure 10. Schematic of the via configuration used for local model (not to scale).](image2)

6. Loading and Boundary Conditions

Assuming that the entire structure reaches the processing temperatures, the stresses and strains that develop within the HDI vias are a direct consequence of the CTE mismatch between the materials under the thermal loading as it is cooled down to room temperature. The work done by most researchers assumes that the entire structure is stress-free at room temperature and determines the operational life by simulating subsequent thermal cycling. Such a stress-free assumption is likely to lead to misleading predictions. To account for the process-induced stresses, the models used in this study simulated the cooling of the polymer layer from the cure temperature to room temperature (25 °C), and the cure temperature was assumed to be the stress-free temperature. The single-step curing process model employed in this work is known as the frozen-view model. The frozen-view model does not account for the complete stress history during the sequential build-up of several thin film layers and, therefore, is less accurate than the sequential process model, as
discussed by Dunne and Sitaraman. After simulating the one-step cure process, at least one model was subsequently subjected to the -40 °C to 125 °C temperature cycling to determine the fatigue life of the vias. This temperature cycle, JESD-22 method A104, accounts for extreme service conditions of electronic packages for commercial applications.

The boundary conditions applied to the global models are shown schematically in Figures 5 and 8. The single-sided geometry is symmetric about the y-axis. Therefore, only one-half of the geometry is modeled, symmetry boundary conditions were applied along the left edge, as shown in Figure 5. In addition, rigid body constraints were placed at the origin of the global x-y coordinate system shown in Figure 5. For the double-sided case, only one-quarter of the geometry was modeled with the bottom edge constrained against vertical displacements and the left edge constrained against horizontal displacements, as shown in Figure 8. It should be pointed out that the thickness of the base substrate layer in the double-sided case remained the same as the base substrate layer in the single-sided geometry. For the local models, the displacements along the left and right cut-boundaries were specified using the deflections of an appropriate set of nodes in the global model.

In all cases, plane-strain constraint with respect to the width (z-direction) was assumed, such that, \( g_{xz} \) = \( g_{yz} \) = \( g_{zz} \) = 0. As mentioned earlier, it was further assumed that the structures were stress-free at the cure temperature of the polymer dielectric, and that the thermal stresses develop as the structure is cooled to room temperature. The structures were also assumed to be devoid of process-induced defects such as voids, microcracks, and non-planar surfaces. Uniform copper plating was assumed based on cross-sectional view shown in Figure 11. It is pointed out that this may not always be the case, as shown in Figures 12 and 13, which illustrate wall tapering and pinching of the corners, respectively. Studies of such vias with process-induced defects are currently underway.

7. Numerical Models

The single- and double-sided HDI structures were discretized using eight-noded quadratic isoparametric plane-strain elements. In the global models, the HDI layers and the base layer contained two rows of elements through their respective thickness (Figure 5), and contained 100 elements along the length of the structure. A mesh convergence study was conducted by increasing the number of element rows through the thickness of the base layer from 2 to 8, and by increasing the number of element columns along the length from 100 to 1250. Figure 14 illustrates the warpage results for the various cases. For this study, the base substrate was a 0.5mm thick Copper-Invar-Copper (CIC) alloy. Based on the convergence study, it was determined that two elements through the individual layers and 100 elements along the length of the structure were sufficient to accurately compute the displacements of the global mod-

Figure 11. Micro-section of a via after temperature cycling.

Figure 12. Micro-section of a double-sided via structure (non-uniform plating thickness).

Figure 13. Micro-section of a via with pinched corners.
Figure 14. Warpage versus mesh refinement.

The local models to study the effects of the via wall angle contained a combination of eight-noded quadrilateral and six-noded triangular isoparametric plane-strain elements. The mesh in the base layer was biased vertically toward the HDI layers. A coarse mesh was used in the regions sufficiently far from the three longitudinally staggered inner vias. The regions between the outer and the inner vias were biased longitudinally towards the inner vias, as the material, the geometry, and the process parametric studies were conducted using the inner vias that are sufficiently away from the cut-boundary edges. The bottom of the vias was divided into two segments that were each biased from the center out. This allowed a fine mesh at the corners of the via walls and in the center of the via. It was ensured that the tractions were continuous across dissimilar material interfaces.

8. Model Validation

The results from the numerical models were verified using two approaches. The warpage values from the global models were compared to closed-form predictions from a laminated plate theory analysis of multilayered structures. Also, the prediction of the fatigue failure using results from the local model was compared to the corresponding experimental data.

8.1. Laminated Plate Theory Analysis

The laminated plate theory presented here accounts for the thermally induced axial stresses due to the CTE mismatch in the various layers through equivalent mechanical loads and moments applied at the mid-plane of the structure on a per-unit-width basis. Edge effects are not included, and the theory does not predict interfacial peel or shear stresses near the free edges. The following relationship between the mid-plane strains and curvatures and the equivalent forces and moments has been widely accepted, Reference11,

\[
\left[ \begin{array}{c}
\varepsilon_x^0 \\
\varepsilon_y^0 \\
\varepsilon_{xy}^0 \\
\rho_x \\
\rho_y \\
\rho_{xy}
\end{array} \right] = \left[ \begin{array}{cc}
[A] & [B]^{-1} \\
[B] & [D]
\end{array} \right] \left[ \begin{array}{c}
N_x^T \\
N_y^T \\
0 \\
M_x^T \\
M_y^T \\
0
\end{array} \right]
\]  

where \(\varepsilon_x^0, \varepsilon_y^0, \) and \(\varepsilon_{xy}^0\) are the mid-plane axial strains in the x and y directions and shear strain, respectively, and \(\rho_x, \rho_y,\) and \(\rho_{xy}\) are the bending curvatures with respect to the x and y directions and twisting curvature, respectively. Also, \([A], [B],\) and \([D]\) are 3x3 matrices whose components are the axial, the coupling, and the bending rigidities, respectively, commonly employed in laminated theory analyses. In the above equation, \(N^T\) and \(M^T\) refer to the equivalent mechanical normal forces and moment per unit width in the x and y directions induced by the thermal loading, and are given by the following relations,

\[
N_j^T = \sum_{i=1}^{n} \int_{y_i}^{y_{i+1}} Q_{ij} \alpha_i \Delta T dy = -\sum_{i=1}^{n} Q_{ij} \alpha_i \left( y_{i+1} - y_i \right) \Delta T \quad (j, k = x, y)
\]

\[
M_j^T = \sum_{i=1}^{n} M_{ij} = -\int_{y_i}^{y_{i+1}} Q_{ij} \alpha_i \Delta T y dy = -\sum_{i=1}^{n} Q_{ij} \alpha_i \left( \frac{y_{i+1}^2 - y_i^2}{2} \right) \Delta T \quad (j, k = x, y)
\]

In equations (2) and (3), \(Q\) refers to the generalized elastic modulus, \(\alpha\) is the CTE, and \(\Delta T\) is the applied thermal load. The superscripts and subscripts \(i\) refer to quantities associated with the \(i\)th layer of the multilayered structure numbered from the bottom. Specifically, \(y_i\) and \(y_{i+1}\) refer to the \(y\)-locations from the geometric mid-plane of the multilayered structure of the bounding interfaces for \(i^\text{th}\) layer, as shown in Figure 15.

Figure 15. Schematic of a multilayered structure for laminated plate theory analysis.

The radius of curvature, \((\rho)_{le}\), of the HDI structure from the Finite Element analysis was assumed to be constant and was calculated from the deformed geometry to be of the form,

\[
(\rho)_{le} = \frac{\delta^2 + \left( \frac{L}{2} \right)^2}{2\delta}
\]
where $\delta$ is the maximum out-of-plane $y$-displacement and $L$ is the total length of the HDI structure. It is assumed that the total length of the board remains unchanged, and that $\delta \ll L$.

Although the laminated-plate theory approximation is a simplified representation of the actual HDI structure, the global warpage values obtained through such an approximation can be used to verify the numerical results from an order-of-magnitude standpoint. When compared against the value obtained using the laminated plate theory (equation (1)), the radius of curvature determined from numerical models (equation (4)) had only a 2.1% difference for the ceramic case and a 1.8% difference for the Cu-Invar-Cu case. It should be noted that the laminated plate formulation outlined above is limited to structures having isotropic and temperature-independent material properties, and therefore, the numerical results for FR4 substrate were not used for the comparison.

### 8.2. Experimental Verification

Results from the Finite Element analysis of this work were also compared to experimental data from 1000-hour thermal cycling tests obtained from an automotive electronics company. There were three different circuit types tested with four boards of each type examined. The double-sided board had 430 vias on each side. The via diameters ranged from 5 to 10 mils (127 to 254 $\mu$m), the via wall thickness ranged from 0.3 to 1.8 mils (7.6 to 45.7 $\mu$m), and the dielectric layer thickness ranged from 1.7 to 3.0 mils (43.2 to 76.2 $\mu$m). The test comprised of -40 to 125 °C temperature cycles with a ramp time of 5 minutes between extremes and with a 25-minute dwell at each extreme. Electrical resistance was monitored with a glitch detector and failure was assessed as a 10% increase in resistance.

The Finite Element models used in this study employed time-dependent behavior of the materials, and therefore, the effects of the ramp rate and the dwell time were not considered. Starting with the cure temperature, the structure was cooled to room temperature, cycled twice through the -40 to 125 °C temperature range, and was then brought back to room temperature. The local geometry for the validation model is given in Figure 16. There were four samples subjected to thermal cycling. Each board contained 430 vias per side. Of the 3440 total vias, only one failure was observed within the 1000-hour temperature cycling based on the electrical resistance.

The calculated fatigue life of the via structure represented in Figure 16 using the above equations was about 108,000 cycles. Caution must be exercised in comparing the theoretical predictions with the experimental data. The theoretical models, although an improvement over several existing models, still need certain enhancements: time-dependent material properties need to be accounted for; full sequential process model along with process-induced defects needs to be included. Also, the fatigue-life prediction model is based on strain-range and empirical in nature. In spite of the shortcomings, the models nevertheless indicate that the via structures are capable of exceeding well over 1000 cycles. The experiments, although stopped at 1000 cycles, seem to indicate that the actual life could be significantly more, as practically none of 3440 vias cracked during the thermal cycling.
9. Discussion and Summary

There has been limited work conducted to-date on the modeling of thermomechanical reliability of HDI structures with vias. Due to the geometric intricacies of the HDI structures, it is apparent that the analysis of real-life detailed HDI structures may be computationally intensive and cumbersome. In light of this, the present work provides a fairly compact and efficient global-local modeling scheme that is expected to yield accurate results while requiring limited computing resources and time.

Past research on HDI structures has assumed the fabricated structures to be stress-free at room temperature. Thermomechanical stress analysis using such an assumption is expected to yield misleading results. In this study, attention is focused on the fabrication of the HDI structure, and a frozen-view model is implemented to simulate the curing of the dielectric layers and cooling the structure to room temperature from the stress-free cure temperature. The results in terms of displacements and fatigue life predictions from the global and local models were found to be in agreement with estimates from laminated plate theory and appropriate experimental data, respectively. Ongoing work in via modeling is aimed at extending the global-local modeling scheme to include the accurate modeling of the entire fabrication process, instead of the frozen-view approach adopted in this work. It is also important to understand the effects of appropriate time-dependent thermomechanical properties of the materials comprising the HDI structures.

The global-local model outlined in this work has been used to study the impact of various parameters such as the material properties, the geometric, and the processing parameters on the reliability of the vias in typical HDI structures. The results from such a study have been published elsewhere. Based on these results, some preliminary recommendations have been made for the screening of geometric designs and selection of materials for the HDI structures prior to prototyping and reliability testing.

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