The Impact of KGD and Module Repair on Multichip Module Cost

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Abstract

The impact of known good die (KGD) probability on multichip module (MCM) yield and cost has been modeled and systematically analyzed. The current work extends the researchers’ previous MCM modeling effort involving single chip populations (a single KGD probability) to modules containing complex, multiple chip populations. Most of the analysis is performed on modules with dual populations (that is, two chip types). In order to develop a total cost picture for an MCM versus the respective KGD probabilities of the underlying chip populations, it was necessary to develop new algorithms to calculate the number of modules necessary to ensure one working MCM, the chip cost as a function of KGD, and chip repair cost as it relates to the complexity of module testing and the actual removal and replacement operations. The combination of these models and algorithms produces cost surfaces in dual (KDG) probability space that contain optimum or minimal points. Associated with the cost minimums are specific KGD probabilities for each chip type in the population. Thus, one only pays for improved KGD probability up to the values that minimize the overall module cost. Repair has a direct impact on the overall module yield and cost. The authors have shown that the first repair makes the most significant improvement in yield and cost reduction. Higher numbers of repairs also have positive impact in large modules. In the dual-population case, there is an optimum number of repairs to minimize cost, and as repair costs increase; this optimum number appears to decrease.

Key words:
Known Good Die, KGD, MCM Cost, MCM Repair, Multichip Modules, and Multiple Population MCMs.

1. Introduction

The production of working Multichip Modules requires the confluence of three major elements: known good substrates, known good chips (or dice), and appropriate assembly processes (defect free). Substrate validation is usually accomplished by a series of design rule checks to ensure compatibility with the fabrication processes followed by substrate electrical testing (using bed of nails or flying probe-type testers) to verify that all the electrical networks on the substrate are connected in the appropriate manner (consistent with the design) and that there are no opens or shorts. Known good die (KGD) requires testing of the chips or die prior to assembly. Much time and effort have been expended on the mounting of die for full functional testing (at speed and temperature) and then demounting them for attachment to the actual MCM part. Following assembly (defect free substrate populated with KGD), the resultant MCM must be tested to ensure a working module, thus, validating the defect-free nature of the assembly process. In an MCM part, if one die fails, the whole module is typically useless, or performance is so reduced that the MCM cannot be sold for its intended purpose or at a price consistent with full cost recovery. Since chip pre-testing
cannot ensure that all dice will perform as planned after assembly, one must either build MCMs so inexpensively that they are throw-aways (that is, using a high-yielding process driven by a large commodity market), or one must be able to repair or replace defective die. Testing to find the defective chips is a key element in the repair process. Without appropriate testing, repair is extremely costly or cannot be performed at all. MCMs must be designed in the beginning for repair, including the complete test matrix and protocol to locate defective die. The need to repair and influence substrate design requiring extended pads; room for die attach and removal collets; robust board metallizations; and, perhaps, extra test points, traces, and/or chips to support the testing process. The chips themselves may need to include extra circuit elements and paths to facilitate the testing process. The design of both substrates and integrated circuit chips for testability is beyond the scope of this work.

This study focuses on the repair issue with the assumption that the defective chips can be located, removed, and replaced, thus producing working modules. The researchers have accounted for the difficulty in locating and replacing defective chips by a repair complexity factor, which relates directly to the cost of these operations. The approach is based on minimizing overall chip and module costs as a function of KGD probability and the number (and associated cost) of repair. Results are shown to be extremely sensitive to the KGD cost model and the relative repair cost of a defective die (that is, finding the defective die and replacing it with a working equivalent).

In previous work, the authors concentrated on modules whose chips all have the same KGD probability. In this current work, the focus was on modules containing chips of different KGD probabilities. Results are presented for different chip populations containing various numbers of chips with different KGD probabilities. Analyses are presented for several cost models and repair scenarios and for various MCM module types. In addition, attention is paid to the estimation of the number of modules required to ensure the production of at least one good module, as well as to refinements (over previous work) in both the chip cost and the repair cost algorithms. Graphical display of the data allows readers to make trade-offs between KGD probability and the cost of both chips and modules. Current results reinforce many of the trends developed in previous studies, but they also provide new insights as to break-even points, both on repair and on spending money for known good die.

2. Definitions and Equations

To quantify the magnitude and impact of repair on the ultimate cost of MCMs, one must introduce a systematic look at MCM yield and the influence of repair on this yield. Since multiple chips with different KGD probabilities complicate the mathematics to some degree, a review of the equations is first introduced and result for MCMs containing chips with a single KGD probability, and then extension of these results to the case of modules having chips with multiple KGD probabilities is achieved.

Single KGD Probability. First let \( P_i(g) = \) probability that \( g \) chips out of a lot of \( n \) chips are good. Assuming that the chips follow a binominal probability distribution, one can write,

\[
P_n(g) = \frac{n!}{g!(n-g)!} p^g q^{n-g}
\]

where,

\[
p_i = \text{probability that an individual chip is good and,} \\
q_i = (1 - p_i) \quad \text{is the probability that an individual chip is bad.}
\]

To find the yield of an MCM containing \( n \) chips without repair, one needs to find the probability that all dice are good. This relation is given by the following,

\[
Y_0^mcm = P_n(n) = p^n
\]

where the zero superscript indicates zero defects or no need for repair in this module.

To find the yield number under repair, one may look for modules with defects less than or equal to the number of repairs, \( r \), per module to make. In previous work, the authors derived a generalized expression for MCM with \( r \) repairs. This expression is given by the following,

\[
Y_r^mcm = P_n(n) + P_n(n-1) p + ... + P_n(n-r) p^r,
\]

\[
= p^n \left[ 1 + n(1-p) + ... + \frac{n!}{r!(n-r)!} (1-p)^r \right]
\]

where \( Y_r^mcm \) is the fractional yield of an \( n \)-chip MCM (all dice having the same KGD probability) with \( r \) repairs, assuming that the repairs of chips themselves have the probability, \( p_c \), of being good. The yield for any number of repairs, \( r \), can be built from the expression on the right-hand size of Equation (3).

Figure 1 plots the MCM yield, Equation (2), as a function of the number of chips in a module for a given probability, \( p_c \), that an individual chip is good. Even at very high KGD probabilities (\( \geq 0.98 \)), large modules containing large numbers of chips still have relatively poor yields (<50%). Figure 2 plots MCM yield with repair (\( r = 0 \) to 5), Equation (3), as a function of the probability, \( p_c \), that an individual chip is good for a 25-chip MCM.
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Figure 1. MCM fractional yield as a function of the number of chips in the module for various chip KGD probabilities (ranges from 0.9 to 0.99).

Figure 2 can be generalized to other sized modules with the observation that the first repair makes the largest percentage improvement in yield, with each succeeding repair diminishing the important1. Similarly, the lower the initial KGD probability, the larger the impact of repair regardless of module size1.

Dual KGD Probabilities. Now, consider a module with n total chips: l chips have KGD probability p1 and m chips have KGD probability p2, where n = l + m. In analogy to the single population case, the yield of this dual-population module with KGD probability p2, where n = l + m. In analogy to the single population case. Figure 3 presents the improvement in MCM module yield (dual population) for the single-repair case. Figure 3 is plotted for various fixed population probabilities as a function of the number of chips of each type in the population. The combined chip population is allowed to range to 100 of each type. For two repairs, the expression becomes as follows,

$$Y^r_{\text{mcm}} = P^*_n(n) + \frac{P^*_n(n-1) + P^*_m(n-2)}{2}$$

(5)

Now, if n = 1, then 2ylm reduces to

$$P^*_n(1) + 2p_1p_2$$

(6)

Similarly, for three repairs,

$$Y^r_{\text{mcm}} = Y_{\text{mcm}}^{n-1} + P^*_n(n-r)$$

(7)

and, in general, for r repairs,

$$Y^r_{\text{mcm}} = Y_{\text{mcm}}^{n-1} + P^*_n(n-r)$$

(8)

where the $$P^*_n(n-r)$$ term takes the form following form,

$$P^*_n(n-r) = p_1p_2 \left\{ \frac{[l-1]...\left(1-p_1\right)}{r!} \right\}$$

(9)

where the asterisk (*) indicates population weighting. The 0 superscript represents no repair and the preceding 2 as a subscript indicates a dual-chip population.
Figure 3 illustrates the increasing effect of the number of repairs on module yield for the dual-population case. For fixed chip population probabilities, the yield is plotted as a function of the number of chips of each type (Type 1 and Type 2) and the number of repairs \( n_r \) \((r = 0, 1, 3, \text{ and } 5)\). Figure 4 plots the MCM yield (fixed dual population, 30 chips Type 1 and 70 chips Type 2) as a function of KGD probability for each chip type and the yield \((\text{fixed dual population, 30 chips Type 1 and 70 chips Type 2})\) as a function of KGD probability for each chip type and the number of repairs \( n_r \) \((r = 0, 1, 3, \text{ and } 5)\). Figure 4 illustrates the increasing effect of the number of repairs on module yield for the dual-population case. For fixed chip population probabilities, the yield is plotted as a function of KGD probability for each chip type and the number of repairs \( n_r \) \((r = 0, 1, 3, \text{ and } 5)\).

Multiple KGD Probabilities. In general, the yield for any MCM containing more than two distinct chip populations can be developed in an analogous manner using the method described above for the dual population case. Thus, for a module containing \( n \) chips composed of \( i \) distinct populations \((1, 2, 3, \ldots, i)\) or KGD probabilities with \( \alpha \) chips of population 1, \( \beta \) chips of population 2, \( \gamma \) chips of population 3, and \( \rho \) chips of population \( i \), such that \( \alpha + \beta + \gamma + \ldots + \rho = n \), the module yield with no repair is given by the following.

\[
Y_{\text{mcm}}^{\text{i}} = P^*_{\text{a}}(n) = p^*_{1} p^*_{2} p^*_{3} \ldots p^*_i
\]

In the case of one repair, again, with repair chips having the same KGD percentage as their respective subpopulations, the MCM yield is given by the following,

\[
Y_{\text{mcm}}^{\text{i}} = P^*_{\text{a}}(n) + P^*_{\text{a}}(n-1)
\]

\[
= p^*_{1} p^*_{2} p^*_{3} \ldots p^*_i [1 + \alpha (1-p_{1}) + \beta (1-p_{2}) + \gamma (1-p_{3}) + \ldots + \rho (1-p_{i})]
\]

and the general term for repairs can be built as for the dual population case using the relation,

\[
Y_{\text{mcm}}^{\text{i}} = P^*_{\text{a}}(n) + P^*_{\text{a}}(n-1) + \ldots + P^*_{\text{a}}(n-r).
\]

In the rest of this paper, the authors will focus on the dual-population case, comparing results to the previously published uniform or single population case.

3. Number of Modules

In the preceding section, the authors calculated MCM module yield for various chip populations and KGD probabilities and showed that module yield is lower for modules with increasing numbers of chips or decreasing \( p_s \) for fixed chip populations. In practice, rather than module yield, one would like to know how many modules, \( N \), must be built to assure selves of at least one working module. There are several ways to derive an estimate of this number. In previous work\(^1\), the authors assumed a defect “rate” model based on the minimization of the probability associated with producing an entirely defective module (all chips are bad). In this current effort, the researchers adopt a confidence level approach\(^3\) for determining \( N \). Since \( N \) varies with chip yield, a general equation for \( N \) can be written as follows,

\[
N = \mu_N + Z_c \sigma_N
\]

where \( \mu_N \) is the average of \( N \), \( \sigma_N \) is the standard deviation of \( N \), and \( Z_c \) is the confidence coefficient\(^1\), which determines the level of confidence in the resulting estimate of \( N \). Values of \( Z_c \) for various confidence levels are given in Table 1.
Table 1. Confidence coefficients Zc for various levels of confidence.

<table>
<thead>
<tr>
<th>Confidence Level *</th>
<th>Zc</th>
<th>Confidence Level *</th>
<th>Zc</th>
</tr>
</thead>
<tbody>
<tr>
<td>50%</td>
<td>0.6475</td>
<td>95%</td>
<td>1.960</td>
</tr>
<tr>
<td>60%</td>
<td>0.8415</td>
<td>96%</td>
<td>2.054</td>
</tr>
<tr>
<td>70%</td>
<td>1.0365</td>
<td>97%</td>
<td>2.170</td>
</tr>
<tr>
<td>80%</td>
<td>1.2815</td>
<td>98%</td>
<td>2.326</td>
</tr>
<tr>
<td>90%</td>
<td>1.645</td>
<td>99%</td>
<td>2.575</td>
</tr>
</tbody>
</table>

*For confidence levels not given in the table, the values of Zc can be found using a normal curve area table.

To determine N, the values of μN and σN must be known. To calculate μN and σN, one assumes that the number of modules that work, out of the number of modules built, N is described by a binomial distribution (consistent with our original probability and yield distributions.) This gives the following,

\[ \mu_w = \mu_N Y = 1 \]  \hspace{1cm} (14)

\[ \sigma_w = \sqrt{\mu_N (1-Y)} = \sqrt{(1-Y)} \]  \hspace{1cm} (15)

where \( \mu_w \) is the average number of modules that work out of the N built. By definition of N, this is equal to 1, and \( \sigma_w \) is the standard deviation of the working modules built from N. Now, if \( \mu_w \) changes by one standard deviation, so will \( \mu_w \). Thus,

\[ \mu_N + \sigma_N = (\mu_w + \sigma_w)/Y \]  \hspace{1cm} (16)

with \( \mu_w = 1, \sigma_w = \sqrt{(1-Y)}, \) and \( \mu_N = 1/Y \); then Equation (16) can be solved for \( \sigma_N \) as follows,

\[ \sigma_N = (\sqrt{(1-Y)}/Y) \]  \hspace{1cm} (17)

and the equation for N (Equation (13)) becomes,

\[ N = 1/Y + Z_c(\sqrt{(1-Y)})/Y \]  \hspace{1cm} (18)

Figure 5 plots this relationship for 90%, 95%, 99%, and 99.9% confidence levels. The expectation value or average value of N (=1/Y) is also plotted for comparison, along with the N found using the previous defect “rate” method with D = 0.05 (or 95% confidence.)

It is interesting that the estimate of N for the previous defect “rate” method compares quite favorably with those from this new method. Just as before, high confidence levels (lower defect rates) require building more modules, while for a given confidence level, higher chip KGD probability decreases the number of modules required.

4. Known Good Die Probability

Many researchers have tried to assess semiconductor die yield and determine what is reasonable to expect for the probability that a chip once received (either from the manufacturer or distributor) is good. A survey of over 25 sources yielded KGD probabilities in the range of 0.5 to 0.99. In this study, the range of KGD probabilities was limited to 0.9 and above. At a KGD probability of 0.9, even small modules (a few chips) suffer significant yield loss (of the order 35% for 4 chips, 52% for 9 chips); thus, considering values below 0.9 does not seem prudent or cost-effective. One would also recognize that for large MCM modules (50 chips and above), the value of the KGD probabilities required is greater than 0.95 to produce a significant (cost-effective) module yield.

Just as additional testing has been used to improve the confidence that the customer has in die quality (that is, KGD probability), improvement in module screening methods can also ensure higher delivered module yield. In fact, confidence that a delivered module (that is, one that has passed manufacturer screening tests and been shipped to the customer) will work when received (assuming it was built with n chips of KGD probability p) is directly related to confidence that the module screening test will detect faults. The representation of this final yield is given by the following,

\[ Y_{mcm} = Y_0^{(1-\eta)} = p_\epsilon^{(1-\eta) n} \]  \hspace{1cm} (19)

where \( \eta \) is the fault coverage percentage of the module test containing a single population expressed as a decimal.
For the two-population case, the expression becomes,

\[ Y_{\text{mon}} = Y_{\text{mon}}^1 (1 - \eta_1) \eta_2 = p_1 (1 - \eta_1) \eta_2 \]  

(20)

where \( \eta_1 \) is the fault coverage percentage for defects in chip population 1 (containing \( l \) chips) and \( \eta_2 \) is the fault coverage percentage for chip population 2 (containing \( m \) chips). An expression for any number of subpopulations can be built in an analogous manner.

Thus, screening can improve confidence that chips or modules that pass the screening tests and are delivered to customers are more likely to work than their unscreened counterparts. However, this screening is difficult and usually very costly. Ideal KGD screening would be to burn-in and test the chip at wafer level; but contact issues, power distribution, and thermal transfer problems make this difficult and costly. Built-in self-test and boundary scan methods have helped this process. At the module level, fault diagnosis and failure isolation are difficult and costly, and the cost increases nonlinearly with chip number and input/output density. Rework costs at the module level are strongly dependent on this test cost, as well as on replacement chip cost and the cost of old die removal, site preparation, and the placement and interconnection of the new die. If this cost is low compared to other module costs, including the cost of KGD, repair is viable. If it is extremely high, all steps must be taken to ensure first product yield, including paying for KGD percentages. Quantification of these concepts is pursued in the following sections.

5. Chip Cost Models

In previous analyses, the authors described various KGD cost models. For this study, they settle on the cost model given by the following relation,

\[ C = C_o \left[ 1 + \alpha \frac{(p_c - p_e)}{(1 - p_e)} \right] \]  

(21)

where \( p_c \) is the KGD probability associated with a known cost \( C_o \) and \( \alpha \) is the scaling constant (typical value 0.33). This expression closely mimics the original cost model at low KGD probabilities, where little premium is paid for improvements in KGD value, but provides strong cost weighting on KGD value improvement at high KGD probabilities, where complete testing costs are extremely expensive. Other cost models can be developed, but the authors believe the one presented in this case is representative of the actual costs encountered in the purchase of KGD and the perceived costs that would be encountered if such dice were available. In the following sections, all calculations are done with a cost model of the form given in Equation (21).

6. Module Repair Costs

Cost of repair is strongly dependent on the ability to locate one or more defective chips in a module containing \( n \) chips. Once the defective part is located, it must be removed, the site prepared for the acceptance of a new die, and the new part attached and interconnected. In developing a model for repair, it has been assumed that the cost of locating the defective dice is dependent on module type (digital, analog, etc.), the number of module inputs and outputs (I/O), the number of die in the module, and a complexity factor that relates to individual die I/O. Similarly, the repair operations themselves relate to the size of the die, the type of die attach used, the number and type of interconnections, and, of course, the number of actual repairs conducted on a given model. Analytically, this repair model is given by the expression,

\[ C_r = m \left[ n_{a1}(c_{\text{rev}} + c_{\text{prep}} + c_{\text{ICCI}} + C_{\text{ICCI}} + \Delta) \right] + \left[ n_{a2}(c_{\text{rev}} + c_{\text{prep}} + c_{\text{ICCI}} + C_{\text{ICCI}} + \Delta) \right] \]  

(22)

Table 2 contains the descriptions and some of the values used in the repair model. Other cost parameters and estimates of module I/O were given previously. Figure 6 illustrates repair costs per module as a function of the number and type of chips in a module and the complexity of repair. Changes in chip and module complexity and density can significantly change these costs. Similarly, the cost of the repair chip is not included in Equation (24), but would be an additive factor to all costs. It is assumed that multiple repair events are essentially independent and that their costs are additive. A multiple repair interaction factor has been added to account for any additional costs (such as damage to adjacent chips or wires).

In handling dual chip populations, the repair model is applied to each type of chip. Thus, a cost of repair is determined for each chip type and then probabilistically weighted based on population statistics and KGD probabilities to determine an average repair cost for a chip in the dual population module.
Table 2. Parameter values for MCM repair cost model.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value or Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>( m )</td>
<td>Number of modules repaired</td>
<td>(a)</td>
</tr>
<tr>
<td>( n )</td>
<td>Number of chips in module</td>
<td>(b)</td>
</tr>
<tr>
<td>( n_R )</td>
<td>Number of repairs per module</td>
<td>0.1 – 5</td>
</tr>
<tr>
<td>( A )</td>
<td>Die area, ( \text{cm}^2 )</td>
<td>0.5 – 5</td>
</tr>
<tr>
<td>( C_{DR} )</td>
<td>Die removal cost, $/cm(^2)</td>
<td>0.5 – 2.5</td>
</tr>
<tr>
<td>( C_{DP} )</td>
<td>Die site preparation, $/site</td>
<td>0.5 – 2.5</td>
</tr>
<tr>
<td>( C_{DA} )</td>
<td>Die attach cost, $/cm(^2)</td>
<td>0 – 2</td>
</tr>
<tr>
<td>( I_c )</td>
<td>Cost per interconnect, $/lead</td>
<td>0 – 0.10</td>
</tr>
<tr>
<td>( C_C )</td>
<td>Cost of repair chip</td>
<td>(d)</td>
</tr>
<tr>
<td>( I_m )</td>
<td>Number of module interconnects</td>
<td>(e)</td>
</tr>
<tr>
<td>( C_{LM} )</td>
<td>Test cost per module lead, $/lead</td>
<td>0.05-0.20</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>Chip complexity factor</td>
<td>1 – 2</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Module complexity (type factor)</td>
<td>1 – 4</td>
</tr>
<tr>
<td>( \Delta )</td>
<td>Multiple repair interaction parameter</td>
<td>(f)</td>
</tr>
</tbody>
</table>

*From confidence interval curves or engineering decision
*User specified
*Chip type, complexity (Rent’s rule [7]), or user specified
*From chip pool, or use cost model
*Rent’s rule, or user specified
*N\(_R\) raised to a power \( \geq 1 \), typically 1.5

7. Total Chip and Module Cost

Total chip cost to produce a working module can be found by combining the various previous elements together (such as number of modules to ensure a high confidence of yield, the cost of chips, and the cost of repair). Figure 6 shows an example of total chip cost for a dual-population module (\( n_1 = 25 \) and \( n_2 = 15 \)) as a function of the KGD probability for each chip type. The Figure illustrates both the no repair case and single repairs of various complexities. As can be seen, the ability to repair significantly influences total chip cost as a function of the respective KGD probabilities. The surfaces plotted in Figure 6 assume that each chip type has unity chip cost at \( p_i = 0.9 \). Figure 7 presents similar data where the small die population (type 2) has a \( C_0 \) that is 10 times larger than that of the larger die population (type 1). The surfaces are complex and the minimums in cost are difficult to locate along the respective probability axes, but it is clear that repair can lower the overall chip costs. Similarly, even though total chip cost for high-complexity repair is larger than for low-complexity repair, even at high cost levels, repair appears to be advantageous, especially as module size increases.

Figure 6. Total chip cost as a function of KGD probability for a dual population module (\( n_1 = 25 \) chips, \( n_2 = 15 \) chips) with 0 and 1 repair. Repairs are classified as low, medium, and high in complexity or cost. Chip costs for both populations are the same.

Figure 7. Total chip cost as a function of KGD probability for a dual population module (\( n_1 = 25 \) chips, \( n_2 = 15 \) chips) with 0 and 1 repair. Repairs are classified as low, medium, and high in complexity or cost. Chip costs for the \( n_2 \) chip populations are ten times larger than the \( n_1 \) population.

To better assess the cost minimums as a function of KGD probability, the authors have developed a two-dimensional, contour mapping approach that locates the minimum cost point in the joint probability plane. An example is shown in Figure 8. The cost minimums are located at the “center” of the innermost contour. This example is for a dual population module (\( n_1 = 25 \) and \( n_2 = 15 \)) as a function of repair (number and complexity). The results indicate a general shift in the minimum location towards
lower KGD probabilities as the number of repairs increases. The only exception exists at high repair costs (complexity) where larger repair numbers seem to require higher KGDs to produce a cost minimum. Table 3 illustrates some of the actual costs associated with these minimum points. Similarly, depending upon chip and repair costs, there appears to be an optimum number of repairs that minimizes the total chip cost, as shown in Table 3 for a typical case. In Table 3, as repair complexity (cost) increases, the optimum number of repairs to minimize cost seems to decrease.

In most cases, for large modules, the total cost for highly complex repair is less than the chip cost without repairs, regardless of repair number. This result contrasts somewhat with the results presented previously for the single-population case for small modules (that is, ≤25 chips).

In extrapolation to total module cost, where chip cost is only a fraction (typically <20%) of the total, the results behave in a similar manner. The higher the additive costs for the other module elements (substrate, initial assembly), the greater the impact of repair. In fact, for substrates with high added value such as MCM-Ds, repair improves yield and saves costs at all reasonable KGD probabilities.

8. Discussion

Most of the results shown in this paper can be generalized to other types and numbers of chips. As can be seen from Figure 2 and Table 3, the first repair improves yield and reduces cost the most. This is true regardless of whether the population is single or dual chip. The authors believe that similar results will hold true for even more complex population distributions. However, as modules get larger, the impact of the second and third repair should not be neglected. With dual-chip populations, depending on relative numbers of chips in each subpopulation, chip cost, and repair complexity, there appears to be an optimum number of repairs to minimize cost; as repair costs increase, this optimum number seems to decrease.

Repair costs are extremely dependent on the ability to locate the defective die. The cost for such tests can vary over orders of magnitude, ranging from tens of dollars for simple modules with a few chips to hundreds and even thousands of dollars for large modules in complex chips. Multiple chip populations can make this problem more difficult. The authors believe the weighted repair model described in this study captures the essential elements and systematically produces costs consistent with actual empirical experience. This cost model produces similar results. The application of the module build number, chip cost, and repair costs models, under most scenarios, has produced cost curves (single-population case) and surfaces (dual-population case) with an optimum (minimum) point or KGD probability(ies). Such minimums suggest that one pays for increased KGD probability(ies) only up to that point.

The ability to repair even after the defective chip(s) is located is a major concern for multichip module producers. Flip Chips should be the easiest to repair of all the first level interconnects. Upon proper controlled and localized heating, the defective die can be
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proper controlled and localized heating, the defective die can be removed from the substrate without substrate damage. Ceramic substrates (MCM-Cs) are the most robust in this regard, followed by Printed Wiring Boards (MCM-Ls), then thin film multilayers such as MCM-Ds. After removal, site clean up and dress is usually required as well as inspection for pad and solder dam damage. Reflow of the new die is accomplished using a localized heat source or hot chuck. If the original die was underfilled, removal is much more difficult and, perhaps, impossible without substrate damage unless reworkable underfill materials were used.

With tape automated bonded chips, both the die attach and the outer lead bonds must be broken and removed. Selective heating can usually remove the outlead bonds, which are typically solder reflowed. The die attach bond (epoxy or metal reflow) can also be removed by applying heat and selective mechanical force. Cleanup and dress of both the outerlead bond pads and the die attach are usually necessary. Again, the robustness of the substrates typically order from ceramic to thin film multilayer.

Wirebonded chips are relatively east to remove, provided they are not glob topped or the glob top is reworkable. Wires can be cut and the dice removed by selective heating and the application of a torquing force. Die attach pad clean up and dress are usually required before installing the new die. The real question is, “Are the pads for the tail bonds large enough to accommodate a second tail bond?” If repair is anticipated, pad size could be increased in the design stage to facilitate repair. If no room exists for a second bond, then an attempt would have to be made to bond over the remaining wire residue (if any) after the old wire has been peeled from the substrate. This may require a tamping operation, followed by tail bond replacement. A security ball can also be used in certain special circumstances. Reverse bonding (ball-on-substrate, wedge-on-chip) has also been observed. The above comments also apply to ultrasonic or wedge-wedge bonding, but no security fall feature exists.

9. Conclusions

The influence of KGD probability on MCM module yield was systematically studied. This work extends previous work to the dual population case and suggests methods for handling even more complex multiple chip populations. Models that estimate module build size, chip costs, and repair costs were developed. Results indicate that the ability to repair MCMs is extremely important and that the repair of at least one chip per module can significantly improve yield. Yield curves or surfaces versus KGD probability(ies) have cost minimums that can be utilized to optimize chip cost and, hence, module cost.

Future work will include expansion to three and four population cases with diverse chips including large numbers of high yield (high KGD probability) passives and a small number of complex, low yielding integrated circuits. Questions to be answered include: “Can passive repair be ignored?”, “Is sequential assembly (and test) prudent and cost effective?,” and “How to know when repair costs are too high?”

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References


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