Thermal Management Using Planarized CVD-Diamond Substrates

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Abstract

CVD diamond (CVD) substrates offer an outstanding solution for various advanced electronic packaging applications such as high power 3-D MCM, laser diodes, and high power MOSFETs. In the manufacturing of such substrates, various post-synthesis processing steps, such as polishing, cutting, and metallization, add significantly to the cost of the package. Recently, the authors introduced a planarization-by-filling process to reduce the cost of polishing and increase the ease of manufacturing. The process involves surface planarization of coarsely-lapped diamond substrates using a filler material such as polyimide, which is regularly used in electronic packaging industry. In the past, the researchers demonstrated successfully the applicability of this planarization process. In this paper, the authors present Finite Element analysis (FEA) and experimental results of thermal management using polyimide planarized CVD substrates, for wirebond and Flip Chip die attachment configurations. Specifically, these results are directed at determining the maximum die temperature for various power densities using liquid convection for edge cooling. Also, the paper presents results of a thermal stress study, using thermal shock, for GaAs laser diodes mounted, using gold-tin hard solder, on a CVD substrate planarized using PI-2610 and 2611 polyimides. It is found that the planarization-by-filling process not only gives an easy and inexpensive solution to the high surface roughness of CVD, but also adds value to the package by providing a compliant layer between the GaAs die and CVD without sacrificing thermal management performance.
CVD Diamond, Thermal Management, Planarization, Thermal Stress, and Laser Diodes.

1. Introduction

CVD diamond (CVDD) is a candidate material for electronic packaging due to its exceptionally good thermal, mechanical, and electrical properties1-3. It can be used as a substrate material for packaging of high power MOSFETs, 3-D MCMs, and laser diodes. For example, advancements in the field of opto-electronics have resulted in generation of high power diode lasers with continuous wave output ranging from 10W up to 60W. These products are being used in various fields, such as space communication, material processing, and medical electronics, among others4-6. Such devices demand efficient thermal management since their performance, optical emission characteristics, decreases drastically with increasing chip temperature7-15.

Typically, as-grown CVDD substrates have a very high surface roughness due to preferred columnar growth, along with randomly arranged poly-crystalline structure and also it has high hardness. The surface roughness limits its immediate applicability as a packaging substrate for example, diamond’s high surface roughness (Ra > 20-50 µm). Thus, planarization of CVDD is necessary if the material is to be used in electronic packaging. Planarization involves either subtractive methods, such as lapping and polishing, or additive methods, such as filling with over-layers of polyimide or metal, or a combination of the two. Achieving an extremely smooth diamond substrate surface using conventional lapping and polishing process is a very expensive and time-consuming step.

Also, the coefficient of thermal expansion of diamond can pose challenge for die attachment, in particular while using hard solders. For example, in the case of laser diode packaging, the CTE mismatch between diamond (0.8-1.2 ppm/°C) and GaAs (5.6-5.8 ppm/°C) leads to an unstable mechanical interface7,15. Nevertheless, due to the tremendous thermal management benefits offered by diamond along with continuously dropping cost of it, efforts continue to be directed at finding solutions to the processing challenges presented by CVD diamond to electronic packaging applications16.

In the past, the authors have successfully demonstrated the concept of diamond substrate planarization-by-filling using polyimide. In this paper, they present results of a parametric thermal management study on such substrates under various ambient conditions. Finite Element analysis (FEA) was performed to predict maximum chip temperature when polyimide planarized CVD diamond is used as a substrate. Experiments were performed to validate the FEA findings. For a thermal stress study, GaAs laser diode dice were attached to polyimide planarized CVDD substrates using Au-Sn hard solder. The samples were then subjected to several thermal shock cycles and examined for die/substrate delamination and substrate and/or die cracking.

2. Finite Element Analysis (FEA)

A FEA model, using ANSYS (version 5.3) was constructed to predict maximum chip temperature for polyimide planarized as well as unplanarized CVDD as a substrate material. These studies were performed on combination of following packaging parameters:

- Wirebond and Flip Chip dice,
- Edge cooled and planarized/unplanarized CVDD substrate,
- For studying and optimizing this edge-cooled CVDD based electronic software.

2.2. Cooling Setup

In determining the proper cooling setup for this work, many methods were considered. For a target power density of 40W/cm², natural air convection is inadequate. Hence, a decision was made to use a combination of natural air and forced liquid cooling. An edge cooling test fixture with an “L” shape was designed to cool the CVD diamond substrate. A channel for liquid coolant was placed 3 mm from the point where the CVD diamond substrate attaches to the fixture using thermally conducting epoxy (‘Ablebond’). A FEA model was constructed for studying and optimizing this edge-cooled setup using ANSYS (version 5.3) software.

Once the model was constructed and meshed, the heat flux and convection coefficients were applied. Heat flux was applied to the top surface of the chip in the case of a wirebonded die. Cooling convection was applied to the inner surface of the liquid channel, and free natural convection was applied to all other external surfaces17. Parameters, such as heat flux and convection coefficient, were varied and the steady-state temperature of the chip was obtained. In order to decrease the time for each run and minimize the cumulative error, the model for the edge-cooled setup was reduced to an equivalent model. In reducing the full model to an equivalent model, one cannot reduce the element count in the FEA model for an edge-cooling setup by modifying nodes near the die, epoxy, planarization layer, or the substrate since it drastically affects the performance of the model. Also, the element count in the cooling block cannot be reduced since this also modifies the heat flow mechanism through the heat sink. It should be noted that fins, although they are very important for cooling, do not take part in convection cooling at low cooling temperatures and high coolant flow. Therefore, if the fins are reduced in such a way that they form an equivalent representation in each section of the heat sink, the problem can be solved much more efficiently. The idea is to simulate the full setup with fins for the highest power dissipation conditions and then eliminate the fins in a systematic way, keeping only one fin per side.
and applying an equivalent convection (number of fins times natural convection coefficient) to achieve the same result. The most challenging condition is when no liquid convection is applied and the maximum heat flux is generated. In these experiments, the heater chip, “PST-2” (Flip Chip Technologies), was operated at 10 W of total power, or 40W/cm².

The parameter, maximum chip temperature, was evaluated for a full model and the result was used as a benchmark. Its value is around 169.391°C. Fine-tuning of the model with strategic placement of fins yielded a maximum chip temperature of 169.4°C. This value is approximately equal to that of the full model, and hence, the reduced model can be considered as a thermal equivalent (Figure 1).

Figure 1. Equivalent reduced model.

2.2. Parameter variation

Parameters, such as chip power (power density), cooling convection coefficient, and cooling temperature, were varied. The cooling convection coefficient was varied from 100 W/m² K to 1000 W/m² K in steps of 100. This range covers low convection (100 W/m²K), medium convection (200-400 W/m²K), high convection (500-700 W/m²K), and very high convection (»1000 W/m²K). The cooling temperature were varied from 0°C to 25°C in steps of 5°C, and the power was varied from 10 W/cm² to 40 W/cm² in steps of 10 W/cm².

2.3. Transient analysis

To obtain the transient response of the model initially, full convection of 250 W/m²K at 10°C was applied to the surface of the liquid cooling channel, which was modeled and meshed like a solid. Natural air convection was applied to the rest of the external area. After a sufficient delay time to ensure that steady-state conditions were reached, the convection coefficient was reduced to zero and the simulation was allowed to continue. The rate of temperature rise was noted and the time required to reach the maximum allowed limit of 100°C was calculated from the graph (Figure 2). This information provides the maximum safe shutdown time for the testing system in the event of that the cooling system fails.

Figure 2. Transient response of edge cooling setup.

3. Experimental Work

CVDD substrates from Norton Diamond Film (Northboro, Massachusetts), having a thermal conductivity of 1000 W/m×K, were used for the experiments. The diamond substrates were lapped and polished to a final surface roughness (Ra) of the order of 0.2 µm. However, surface pits in CVDD can create serious problems during photolithography and metallization processes. Therefore, it is important to fill these pits in CVDD and planarize it. The authors have successfully demonstrated planarization of CVDD using polyimide. The same procedure was applied to planarize the CVDD used in this work. DuPont polyimides 2610 and 2611 were used to planarize the substrates by spin coating 7µm thick layer of polyimide onto them. The process produces excellent planarization of the CVDD surface without adhesion, blistering, or cracking problems. The process is discussed in detail elsewhere. Figure 3(a) shows typical microcavities (or surface pits) in unplanarized CVDD. Figure 3(b) shows CVDD after planarization with polyimide.

Heater test dice were attached and wirebonded to both planarized and unplanarized CVDD substrates. Following die attachment and wirebonding, the edges of the substrate were inserted, following coating with “Ablebond” thermal grease, into a 1mm wide, machined seat in the edge-cooled fixture, for experimental evaluation. Liquid cooling was provided. Once the testing setup was complete, electrical power was provided to the chip. The maximum temperature of the chip for various input powers and cooling conditions was measured by placing thermocouples (J type) at various positions, including one right on the top of the chip. The coolant (water) temperatures at the sump, inlet, and outlet were measured with a thick K-type thermocouple.
The temperature measurement was also performed using a diode chain on the heater die and an IR camera in order to confirm the accuracy of thermocouple temperature measurements at various locations on the chip and substrate. Simulations were performed for five different coolant temperatures (0°C to 25°C), ten different cooling convection coefficients (100 W/m²K to 1000 W/m²K), and for four different power levels (10 W/cm² to 40 W/cm²). Graphs for the experimental results were obtained for each setup using the diode chain voltage of the heater chips to calculate the temperature using the correlation equation obtained from the calibration. From the temperature graph, $R_{thermal}$ for each case was calculated using the backward difference method.

4. Results and Discussion

Thermal modeling of the edge-cooled test structures for unplanarized and planarized wirebond setups were performed.

4.1. FEA Results

4.1.1. Edge-Cooled Unplanarized CVD Diamond in Wirebond Configuration

Figure 4 shows that, for power dissipation of 10 W/cm² at high convection rates (500 W/m²°C), and room temperature (25°C), the chip temperature is between 50-60°C. This can be further reduced either by increasing the convection coefficient (using a high capacity pump) or reducing the cooling temperature (using a chiller). For power dissipation of 40 W/cm², the chip temperature is about 120°C. The surface plots, shown in Figure 4(a) and 4(b), indicate that there are two modes of heat transfer. At higher levels of convection and lower coolant temperatures, the heat transfer is essentially by liquid convection, and hence, the slope is low. For low convection and higher coolant temperatures, free convection is dominant. Hence, the slope is higher.

Figure 3a. Unplanarized CVDD ($R_a = 10\mu m$).

Figure 3b. Planarized CVDD ($R_a = 4.9\mu m$).

Figure 4. FEA results of edge cooled unplanarized CVDD with wirebonded chip for power densities, (a) 10 W/cm², and (b) 40 W/cm².
4.1.2. Edge-Cooled Planarized CVD Diamond in Wirebond Configuration

Figure 5 shows the effect of planarization on maximum chip temperature. At lower power of 10 W/cm², for any value of convection coefficient, the difference in maximum chip temperature for unplanarized and planarized substrates is only about 15°C. This shows that 7µm layer of polyimide does not present a major thermal barrier. At higher power density, this difference increases. However, the increase can be easily compensated either by reducing the thickness of the over layer or by substituting it with high thermal conductivity material, such as diamond-filled polymer or metal.

4.1.3. Edge-Cooled Unplanarized CVD Diamond in Flip Chip Configuration

Similar to wirebond die attach, Flip Chip die attachment case shows two modes of heat transfer. At higher level of convection (500 W/m²°C), and lower coolant temperature liquid convection is dominant, while free convection is dominant at lower convection rates (100 W/m²°C) and higher coolant temperature. Figure 6 shows maximum chip temperature at power density level of 10 W/cm² and 40W/cm² for various convection rates and coolant temperatures.

4.1.4. Edge-cooled planarized CVD diamond in Flip Chip configuration

The simulation results for edge cooled setup with planarized CVD diamond in Flip Chip configuration are shown in Figure 7. Similar to wirebond case, at lower power of 10 W/cm², for any value of convection coefficient, the difference for unplanarized and planarized substrates is only about 15°C.
4.2. Experimental Results

4.2.1. Edge-Cooled Unplanarized CVD Diamond in Wirebond Configuration

Figure 8(a) shows the effect of varying convection for unplanarized (U), wirebonded (W) test structures at 25°C. The convection rates used are 3 GPH, 6 GPH, and 12 GPH. There is no marked difference in maximum chip temperature for any variation in cooling convection. This implies that the liquid convection is the maximum at all levels. It is also seen that the slope at the lower power density levels (<15 W/cm²) is small and at the higher power density levels is high. This is primarily due to the fact that at these power density levels, heat dissipation is more dependent on free air convection. The graph in Figure 8(b) shows the effect of reducing the coolant temperature to 5°C for unplanarized wirebonded die at a convection of 12GPH. At lower power density levels (<15 W/cm²), the reduction in maximum is almost equal to the reduction in coolant temperature, which is expected. This shows that the heat dissipation is more dependent on free air convection at higher power density levels, and less affected by a reduction in coolant temperature. The average thermal resistance (R_{thermal}) is 3.48°C/W.

4.2.2. Edge-Cooled Planarized CVD Diamond in Wirebond Configuration

The experimental results prove the FEA findings for planarized substrates. It is seen that there is very little effect due to variations in the flow of liquid (Figure 9(a)). The curve exhibits a slope change similar to what is observed for unplanarized substrates. Reducing the coolant temperature yields an almost proportional reduction in the maximum temperature as can be seen in Figure 9(b). The thermal resistance was calculated and the average R_{thermal} is about 3.566°C/W with a standard deviation of 0.734². This is very close to that of the unplanarized case (3.44°C/W).
4.2.3 Edge-cooled unplanarized CVD diamond in flip-chip configuration

Experimental results on the effect of varying convection and reduced coolant temperatures are shown in Figure 10. Experimental results are very close to FEA results except for higher power results (>20 W/cm²). As shown in Figure 10(a) maximum temperature varies with cooling convection. Reduction in cooling temperature reduces the chip temperature proportionally as shown in Figure 10(b). The thermal resistance was calculated and the average $R_{th,serious}$ is about 4.27°C/W with a standard deviation of 1.67. This value is about 24% more than the wirebonded case. This is due to the fact that thermal management in this configuration depends fully on the liquid convection and is insensitive to free convection. This means that a better underfill would be required for better thermal management of Flip Chip.

4.2.4 Edge-Cooled Planarized CVD Diamond in Flip Chip Configuration

Figure 11 shows effect of varying convection and reduced temperature on maximum chip temperature in the case of planarized Flip Chip configuration. Unlike unplanarized Flip Chip configuration, experimental results on planarized ones show no influence of variation in cooling convection on maximum chip temperature. The average thermal resistance for this configuration was found to be 5.387°C/W, with standard deviation of 1.216. This increase as compared to unplanarized Flip Chip configuration is mainly due to inefficient heat transfer through the underfill and also due to addition of planarization layer.
5. Laser Diode Attachment to Planarized CVDD

Although soft solders like In-Pb can be used to provide compliance between GaAs and CVDD, for important reasons such as high mechanical reliability, better creep resistance of the die attach, and high thermal conductivity of hard solders like Au-Sn are preferred. The attachment of GaAs die to a diamond surface using hard solders is one of the major challenges to the routine use of diamond in the packaging industry. One of the objectives of this work was to experimentally determine if a polyimide planarization layer provides any compliance for a GaAs die attached to CVDD. Experiments were conducted by attaching laser diode bars from Coherent Semiconductor Inc. (Santa Clara) to diamond substrates using Au-Sn (80-20) hard solder. Laser diode bars were attached to unplanarized as well as planarized, CVDD substrates. These bars have 19 emitters and operate at a power density of 400 W/cm². The samples were visually and SEM (Hitachi) inspected and subjected to thermal shock testing to obtain initial results on GaAs to diamond adhesion reliability. Thin strips of gold solder dispersed in 90% flux were placed on the substrates and the dice were placed on them. The samples were then subjected to reflow at 365°C in an IR oven under nitrogen ambient. The samples were then inspected with an optical microscope and a SEM. Immediately following the reflow at 365°C, the laser bar on the unplanarized diamond substrate detached from the substrate by breaking away from the die attach interface, whereas, the die on the planarized substrate was intact (see Figure 12). The planarized die, which survived the 365°C reflow, was then subjected to a thermal shock test (-55°C to 120°C). The GaAs sample was observed for micro-cracks after each interval of five thermal shocks. At the end of fifteen cycle, a large number of microcracks on the die surface, along the die thickness, and even in the solder layer were observed (see Figure 13). However, the die did not detach from the diamond substrate. The process was repeated to test for failure reproducibility. The researchers believe that the curvature in the detached die, and the detachment event, are the signatures for major interfacial stress due to a CTE mismatch. Further, the die remained intact on the planarized substrates due to the compliance (CTE of polyimide is ~3 ppm /°C) provided by the polyimide layer. Further work is being conducted on this subject at the present time.

Figure 11. Experimental results of edge cooled planarized CVDD with Flip Chip for (a) various cooling convection rates at coolant temperature of 25°C, and (b) reduced coolant temperature of 5°C.

Figure 12. GaAs diode bars after 365°C reflow, on planarized (top) and unplanarized (bottom) CVDD substrates. Bent die with a new flat die for comparison (right).
6. Summary and Conclusions

The results of thermal analysis show that a 7µm thick polyimide planarization layer on a diamond substrate does not create a significant thermal barrier. It increases the maximum chip temperature by 15°C at lower power level of 10 W/cm² compared to unplanarized substrates in wirebond as well as Flip Chip configuration.

Initial results on GaAs die attached to planarized CVDD using Au-Sn hard solder show that the GaAs dice can successfully withstand a 365°C solder reflow and up to fifteen thermal shocks before microcracks appear on the die surface. These results demonstrate that high power electronic packaging applications, such as packaging of laser diodes, can be realized with CVDD substrates, which have been planarized using polyimide as a filler material. The planarization-by-filling process not only gives an easy and inexpensive solution to the high surface roughness of CVDD, but also adds value to the package by providing a compliant layer between the GaAs die and CVDD without sacrificing thermal management performance.

7. Future Directions

The studies carried out in this work show that it is possible to achieve good thermal management and reduced stress, using polyimide planarized CVDD. In the future, findings of this work can be directly applied to packaging of higher power laser diode applications. This needs, however, more research on finding filler material like polyimide which have higher thermal conductivity and at the same time provide compliant layer to allow hard solder die attachment on CVDD.

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References

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