Board Level Reliability of Chip Scale Packages

Advanced Semiconductor Engineering, (ASE), Inc.
26, Chin 3rd Rd., 811
Nantze Export Processing Zone
Kaohsiung, Taiwan
Phone: 886-7-3617131 ext. 5210
Fax: 886-7-3613094
e-mail: Mike_hung@asek.asetwn.com.tw

Abstract

The joint fatigue life of PBGA, TFBGA, Film BGA, micro-BGA and BCC/BCC++ is studied in this work. The effects of temperature profile, joint standoff, polyimide thickness, epoxy thickness, test board surface finish, and solder paste composition on the fatigue life are investigated. The temperature ramp rate has significant effect on the joint fatigue life. Attention should be paid not to reach the level of thermal shock. The effect of joint standoff can be predicted by shear strain energy density in the joint. The effect of polyimide thickness on the joint fatigue life is found to be more significant than does die paste thickness. The surface finish of test board also influences the fatigue life, although the difference between OSP and HASL is not significant. A 2% silver additive in the eutectic solder paste improves joint fatigue life. Different pad configurations induce different levels of stress concentration, and thus cause different levels of damage. This effect is found the same for both rigid- and flex-BGA. DNP effect is found to be very insignificant for both TF and Film BGA. However, the die edge effect is demonstrated to be tremendous. This can be due to the stress concentration and warpage near the edges of the chip caused by local CTE mismatch and the changes in flexural rigidity. Surface finish of test board affects the formation and the type of IMC. Different IMC affects joint fatigue life differently and cause different failure modes.

Key words:
Chip Scale Package, Film BGA, TFBGA, Micro-BGA, BCC, Fatigue Life, and Reliability.

1. Introduction

As portable electronic devices have become smaller, thinner, lighter, and more powerful in the recent years, the request of chip scale packages has become extremely high. However, since the packages have the characteristics of small and thin outline, and thus fine pitch and high density, the standoff of the solder interconnects becomes lower, the compliance of the solder joints degrades. Furthermore, the volume fraction of the chip in chip scale packages becomes larger, hence intensifies the thermal mismatch between the package and the motherboard. As a result, the fatigue life of the solder joint interconnection is under a great impact due to the smaller pad size, lower standoff height, and greater thermal mismatch. Therefore, the second level reliability becomes a key issue for chip scale packages.

Recently, sizable efforts have been devoted to investigate the board level reliability of chip scale packages. The fatigue life of a wide variety of CSP was reported. The works cover a wide range of package types including rigid substrate CSP, flex substrate CSP, lead-frame CSP and wafer level CSP. The other attempt in predicting joint fatigue life is by evaluating the thermal stress induced in solder joint using numerical models. Using Finite Element modeling, the package design can be optimized prior to package prototyping, however, the drawback is the verification and the validation of these models. Furthermore, process-related factors are difficult to be included into these models. Key factors affecting joint reliability were investigated and discussed extensively for various Chip Scale packages. The factors investigated include die size, pad design, die paste, solder shape, solder composition, underfill, board thickness, and surface finish of test board. As more chip scale packages are to be used in telecommunication products, the joint reliability under mechanical tests such as bend and drop tests are gaining popularity. More recently, a work to discuss field and accelerated test conditions has been reported and
raised a question whether solder joints have been over-designed.

Since assurance of board-level reliability of a package is essential for applying it into products, this work investigates joint reliability of several chip scale packages under thermal cyclic test. The packages are TFBGA (thin and fine pitch), Film BGA, micro-BGA, and bump chip carrier (BCC/BCC++). A small PBGA is also tested as a benchmark. Both of the TFBGA and Film BGA have a die-up, wirebonded and over-molded configuration. TFBGA uses a BT substrate, while Film BGA uses a polyimide substrate. Since the size of TFBGA is only 8mmx9mm with 1.1mm mounting height and 0.75mm ball pitch, it becomes a suitable candidate for flash memory SRAM, ROM, RAM and ASIC. Film BGA has a size of 12mmx12mmx1.1mm and has 132 solder balls with 0.8mm ball pitch. It uses polyimide as a substrate to enhance its electrical and thermal performance. As a result, it is suitable for ASIC, DSP, flash and portable equipment such as cellular phone, digital camera, and digital tape recorder. The size of micro-BGA is 7.8mmx5.8mm with a mounting height of 0.93mm and 0.75mm ball pitch. Its application is aimed at DRAM and flash memory. As for bump chip carrier, normal BCC has a size of 7mmx7mm and 48 terminals. BCC++ has extra ground wires and an extra cavity, which connects to the motherboard after surface mount. Therefore, its electrical and thermal performance is enhanced. Its size is 9mmx9mm with 64 terminals. Both of BCC and BCC++ have 0.8mm mounting height and 0.5mm ball pitch. Their main application is for telecommunication products.

2. Test Vehicles and Experimental Matrix

In this work, the PBGA test vehicle is used to study the effect of temperature profile on the fatigue life and also the die edge effect on the failure location. Two different sizes of solder balls were used for TFBGA, and therefore the effect of joint standoff on the fatigue life is obtained. For the Film BGA, four types of specimens were prepared to probe the effects of epoxy thickness; polyimide thickness and test board surface finish on the joint fatigue life. The package profile, die size, and ball matrix of TFBGA, Film BGA, and PBGA are shown in Figure 1. For micro-BGA and BCC/BCC++, the main goals are to probe the joint fatigue life and the corresponding failure modes under temperature cyclic test due to their special and unique configurations. The cross sections of BCC/BCC++ and micro-BGA are illustrated in Figures 2 and 3, respectively. Also, the package outline dimensions of each test vehicle conducted are summarized in Table 1. Sample size, package parameters, and test board thickness/surface finish are all listed in Table 2.
Table 2. Parameters of test vehicles.

<table>
<thead>
<tr>
<th>Package</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>G</th>
<th>H</th>
<th>I</th>
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<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td>1.6</td>
<td></td>
</tr>
<tr>
<td>Pad finish</td>
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<td>HASL</td>
<td>OSP</td>
<td>OSP</td>
<td>OSP</td>
<td>HASL</td>
<td>HASL</td>
<td>HASL</td>
<td>Ni/Au</td>
</tr>
<tr>
<td>Die size (mm)</td>
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<td>9.0</td>
<td>9.0</td>
<td>9.0</td>
<td>9.0</td>
<td>5.6x7.9</td>
<td>5.3x7.1</td>
<td>4.57</td>
<td>8</td>
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<tr>
<td>Epoxy thickness (µm)</td>
<td>25</td>
<td>75</td>
<td>75</td>
<td>25</td>
<td>25</td>
<td>NA</td>
<td>12.5</td>
<td>12.5</td>
<td>25</td>
</tr>
<tr>
<td>Ball size (mm)</td>
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<td>0.45</td>
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<td>Au thickness (µm)</td>
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<td>0.5</td>
<td>0.5</td>
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<td>0.03</td>
<td>0.75</td>
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<td>Polyimide thickness (µm)</td>
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</tbody>
</table>

3. Experimental Procedures

The procedure of the preparation of test vehicles and experimental setup is described in this section. For each of the test vehicles under investigation, a specific test board is designed. Test board is made of FR-4 and is designed to carry 15 test vehicles simultaneously. The test board has a size of 220mmx139mm with a thickness of either 0.8mm or 1.6mm. The packages under investigation were then assembled using daisy substrates. After package assembly was completed, the packages were baked at 125°C for 24 hours to remove any potential moisture inside the packages. At this point, the test vehicles are ready to be mounted onto the test boards. The procedure of surface mounting is described next. Solder paste was first printed onto test boards, and packages were then mounted onto test boards by the assistance of a fine-pitch pick and place machine. X-ray inspection was performed to ensure that all samples are located at exactly the right positions. Finally, all the test vehicles went through a ten-zone, nitrogen-inert, forced-convection oven for reflow process. The peak temperature of reflow is 220±10°C.

After the packages were surface-mounted onto the test boards, the electrical circuit formed by daisy substrate and test board was examined to assure a good connection of all solder joints, then all the test units were put into a temperature chamber for cyclic testing. Since solder joints of a test unit are daisy-chain connected, a real-time resistance measurement is implemented. The test system includes a control unit, a chamber, and a data acquisition system. The system is capable of measuring real-time in situ electrical resistance of each and every test unit and also recording the corresponding temperature. In the measurement of resistance, four-point probe is applied instead of two-terminal configuration to remove any effect (error) from connectors and wires. Failure criterion is defined as resistance reaches 300 ohms.

The two temperature profiles used in this work are shown in Figures 4 and 5. Each Figure contains prescribed and measured temperature profiles. From these Figures, it can be seen that the measured temperature profiles follow the prescribed ones reasonably well. Figure 6 shows a typical resistance measurement of a daisy-chain unit (test vehicle). The resistance of a unit is initially low and stable for most of the cycles that it is subject to and then becomes higher prior to solder joint failure. The variation of the resistance prior to failure is believed to be caused by the initiation, propagation, and resting of cracks during the temperature cyclic test. The test is stopped after all units on the same test board fail. The recorded failure cycles were used to generate Weibull plots and parts were then subject to failure analysis.
4. Fatigue Life of Solder Joints

In this section, fatigue life obtained of each test vehicle is reported. The effects of temperature profile, joint standoff, polyimide thickness, epoxy thickness, test board surface finish, and solder paste composition on the joint fatigue life are discussed and compared.

4.1. Temperature Profile Effect

Two temperature profiles were used to study their effect on the joint fatigue life. Both of these two profiles have the same frequency of one cycle per hour (cph). However, the ramp-up time, the dwell time at the highest temperature, the ramp-down time, and the dwell time at the lowest temperature are 15, 15, 15 and 15 minutes, respectively, for the first profile, and 5, 25, 5 and 25 minutes, respectively, for the second profile. The temperature range for the first profile is from -40 to 125°C, while the second one is from -25 to 125°C. Therefore, during transition periods, the temperature ramp rates are 11 and 30°C per minute for the first and second profiles, respectively. Both temperature profiles have been shown in Figures 4 and 5.

The PBGA test vehicles were used for this study. The Weibull plots of the joints tested under these two conditions are shown in Figure 7. The characteristic fatigue life of the solder interconnect is 1482 and 755 cycles, respectively, for the first, and the second temperature profiles. It was found that the characteristic fatigue life of solder joints under the first temperature profile is 1.96 times of that under the second one. Although the temperature variation (ΔT) of the first profile is bigger than the second one, the ramp rate and the dwell time of the second one are both severer than the first one. The ramp rate of the first profile is 11°C/min, while it is 30°C/min for the second one. According to the specification of IPC-SM-785, the maximum ramp rate is defined as 20°C/min for thermal cyclic test. Furthermore, a ramp rate of 30°C/min reaches the level of thermal shock by specification definition. Since thermal shock introduces cracks at much earlier stage and, the longer dwell time introduces and accumulates more creep and stress-relaxation-enhanced damage to solder joints, therefore, the joint fatigue life under the second temperature profile is only 51% of the joint fatigue life under the first temperature profile.

4.2. Joint Standoff Effect

TFBGA is used to carry out this effect. Two sizes of solder balls were applied, which are 0.3mm and 0.4 mm. The first failure occurs at 885 and 1716 cycles, respectively, for the two joint standoffs. Again, the characteristic joint fatigue life is 1325 and 2290 cycles for 0.3mm and 0.4mm solder balls, respectively. From Figure 8, a factor of 1.73x is obtained. Since the only difference between the two test vehicles is the joint standoff, the shear strain induced in the joint by the CTE mismatch between the package and the test board is inversely proportional to the standoff. As a result, the strain energy density in 0.3mm ball is about 1.78 (square of 0.4/0.3) times of that in 0.4mm ball. Since the fatigue life is approximately inversely proportional to the strain energy density (Coffin-Mason equation), the fatigue life of 0.4mm ball can then be expected to be 1.78 times of the fatigue life of 0.3mm ball. Since the ratio obtained from experimental result is 1.73, it can be concluded that the experimental result matches the simulated prediction very well.

Figure 6. A typical resistance measurement.

Figure 7. The effect of temperature profile on joint fatigue life.
4.3. Epoxy Thickness/Polyimide Thickness Effect

Three types of specimens, labeled as C, D, and E in Table 2, of Film BGA were designed to investigate the effects of epoxy and polyimide thickness on the joint fatigue life. Specimens C and D with die paste thickness of 25 and 75 microns were used to study epoxy thickness effect. The cumulative failure functions of the joints for each case are shown in Figure 9. The characteristic joint fatigue life obtained from test vehicles with epoxy thickness of 25 and 75 microns is 1783 and 1749 cycles, respectively. The difference in fatigue life is only 2%. Therefore, it is concluded that the effect of die paste thickness on the joint fatigue life for Film BGA is negligible. As for specimens D and E, the effect of polyimide thickness on fatigue life is investigated. Specimen D has a higher joint fatigue life of 1783 cycles compared to 1321 cycles of specimen E. A factor of 1.34x was obtained for this case (Figure 10). Therefore, for a flex BGA, it was found that the package with thicker polyimide (75µm) exhibits longer joint fatigue life compared to the one with thinner polyimide (50µm).

Since the stress induced in the solder joint is due to CTE mismatch between the package and the test board, especially from the mismatch between the chip and the test board. Therefore, the increase of both die paste and polyimide thickness is believed to be able to increase the joint fatigue life by reducing the level of stress in the joint. The reason for that is both the die paste and the polyimide can absorb the displacement induced by the CTE mismatch between the chip and the test board, therefore, the displacement mismatch in solder joints can be reduced if the thickness of the die paste or the polyimide is increased. For this case, this inference was found to be valid only for polyimide, but not the case for die paste. The difference between the two cases could be due to their difference in size. Since the polyimide substrate covers a much bigger area than does the die paste, therefore, the effect from the polyimide on the joint fatigue life is also much more significant than the effect from die paste.

4.4. Test Board Surface Finish Effect

Specimens B and C were designed to study the effect of test board pad finish on the joint fatigue life. Test vehicle B uses HASL-processed test boards, while test vehicle C uses OSP-processed ones. The Weibull plots of the joint fatigue life obtained from the two test vehicles are shown in Figure 11. For the characteristic joint fatigue life, it is 1749 and 1567 cycles for OSP and HASL-processed test boards, respectively. The joint fatigue life obtained due to different board surface processes is close, only 12% is seen between the two specimens. The fact that OSP performs slightly better than HASL in the solder joint fatigue life has been reported previously. A work with more insight into this field is to be presented.
4.5. Solder Paste Composition Effect

This effect was investigated using BCC++ with 64 terminals. Two solder pastes, used for this work, were 63Sn-37Pb and 62Sn-36Pb-2Ag. The cumulative failure function of the interconnect using solder paste with and without silver content is shown in Figure 12. Without silver content, the characteristic fatigue life of the joints is 4020 cycles; while with silver content, it increases to 4956 cycles. This shows that using solder paste with a 2% silver additive increases its joint fatigue life by a factor of 1.23. A similar trend (1.28x) was also found when the PBGA test vehicle was used. When 2% silver additive is added into solder balls, an improvement in joint fatigue life is also reported in previous work. The result obtained in this work is in agreement with previous result, although the silver additive is only for solder paste.

4.6. Micro-BGA and BCC

Due to their special and unique configurations, the joint fatigue life and their failure modes under temperature cyclic test were also probed in this work. Since their sizes are competitive, the characteristic joint fatigue life of the two packages is shown in Figure 13. For micro-BGA, its first failure was found much higher than 1000 cycles, which is the usual requirement in industry. Indeed, the characteristic fatigue life of its solder joints even reaches 1895 cycles. As for BCC package, the characteristic fatigue life of its solder joints (terminals) reaches 3750 cycles, which is much higher than the requirement from industry. Therefore, it can be concluded that, for both micro-BGA and BCC, there are no concerns about their solder joint reliability under thermal cyclic tests.

5. Failure Analysis

Failure analysis of the test vehicles is reported in this section. After the completion of thermal cyclic test, test units of each test vehicle were first sawed off from test boards. The test units were then subject to cross sectioning along each row of solder balls. SEM photos were taken to identify the failure interfaces. Energy dispersive X-ray (EDX) was performed to identify the intermetallic compound (IMC). The details of the failure analysis of each test vehicle are presented in the following categories.

5.1. Pad Configuration Effect

After the completion of the cyclic test, some TFBGA were first peeled-off from test boards. It was found that the solder joints were preferably left on the test board instead of the substrate (Figures 14 and 15). Since there is some leftover solder on the substrate pads (Figure 14), the failure is verified to occur inside the solder balls, not right at the interface between the sol-
der joint and the substrate pad. Clearly, the weakest point of the solder joint of TFBGA is near the interface of the joint and the substrate. The difference between the two ends of a solder joint is its shape. Since the substrate pad configuration is solder mask defined (SMD), the joint on this side tends to have a sharp angle between joint and substrate; while the pad configuration on test board side is non-solder mask defined (NSMD), the pad on the test board is well surrounded by solder joint. The cross section of a typical solder joint is shown in Figure 16. As a result of the difference in pad configurations, the induced stress concentration levels on both sides of the solder joint are also different. On the substrate side, the sharp angle geometry induces higher level of stress concentration. This level of stress concentration does not occur on the test board side since the pad is well covered by solder. The higher stress initiates cracks earlier and thus the damage of the joint is always on the substrate side. Therefore, the solder joints were left on the test boards after the cyclic test.

Similar phenomenon was also observed for a package housed on a flex substrate- Film BGA. The solder joints after thermal cyclic test were again found to left on the test board (Figure 17), not on the package substrate (Figure 18). The cross section of a typical solder joint of Film BGA is shown in Figure 19. It can be concluded that the pad configuration effect on the failure of solder joint is the same for both rigid- and flex-substrate BGA. Similar results were also reported for flex BGA19-20 and in a review paper11. Furthermore, the same situation for PBGA and Micro-BGA is true. The cross sections of these two packages are also shown in Figures 20 and 21, respectively. The cracks were both seen near and along the interfaces of the substrate pad and the solder joint. As for BCC and BCC++ packages, the theory is different. Since on the lead-frame side, the terminal is well surrounded by solder similar to the case of the test board pad, the stress concentration found in BGA-type packages does not exist in this case. As a result, the failure occurred inside the solder joint and there is no preference for the crack to initiate and propagate near the package terminal. Cross-sectional photos of BCC and BCC++ are shown in Figures 22, and 23, respectively.
Figure 18. Only a few solder joints are left on the substrate after cyclic test (Film BGA).

Figure 19. The cross section of typical solder joint after tests (Film BGA).

Figure 20. The cross section of typical solder joint after tests (PBGA).

Figure 21. The cross section of typical solder joint after tests (micro-BGA).

Figure 22. The cross section of typical solder joint after tests (BCC).

Figure 23. The cross section of typical solder joint after tests (BCC++).
5.2. Chip Effect

Since the chip has the smallest coefficient of thermal expansion (3ppm) of a package, the effective CTE of a package is greatly affected by the size of chip. This effect can be demonstrated reasonably through Moiré fringe patterns. Shown in Figure 24 is a Moiré fringe pattern of Film BGA. From this picture, it is clear that the difference in in-plane deformation is so significant for the areas inside and outside the chip size. Similar phenomenon was also noticed for a lead-frame package-BCC (Figure 25). As a result, due to the effect of chip, the part of the solder ball near the package side is constrained to deform during a thermal cyclic test, especially for the solder balls directly under the chip. However, the test board has a much higher CTE (17ppm) and would like to deform more as temperature increases during thermal cyclic test. As a result, the solder joints are under a condition of shearing. The induced shear stress is a key factor for damaging the solder joints. The displacement mismatch (resulted from CTE mismatch) increases as the distance from the neutral point (DNP) of the package increases. Therefore, the solder joints at longer DNP usually suffer relatively severe damage than those at shorter DNP. This is the so-called DNP effect and is usually observed in ceramic packages.

For TFBGA, every solder ball of a test vehicle was checked row by row using cross sectioning. It was found that the damages to the solder balls near package edge (Figure 26) and in central region (Figure 27) are approximately the same. In other words, no DNP effect was observed for TFBGA. It is believed that this is due to the low flexural rigidity of BT substrate compared to the ceramic one. The warpage induced during temperature cycling may cause severe damage to the solder joints than the effect of DNP. As for Film BGA, again, the DNP effect was not found in this case since the damage to the solder balls at different locations is approximately the same. The reason for that is again due to the extra low flexural rigidity of the polyimide substrate used for Film BGA. Since the polyimide substrate is so flexible, the ball pad is even bended after temperature cyclic test (Figure 19). Therefore, the warpage introduced during temperature cyclic test for Film BGA can be expected to be relatively severe than that for TFBGA. The damage to the solder joint associated with the warpage could override the DNP effect. It can be concluded that for both rigid- and flex-type BGA, the DNP effect does not exist or is insignificant.

Figure 24. Moiré fringe pattern of Film BGA.

Figure 25. Moiré fringe pattern of BCC.

Figure 26. Solder joint near package edge (TFBGA).

Figure 27. Solder joint in the central region of a package (TFBGA).
5.3. Die Edge Effect

For the PBGA test vehicle, as shown in Figure 28, the daisy circuit is divided into six loops. In such a way, the joint failure in each loop can be examined separately. After the test is completed, each loop was checked to see whether joint failure occurred inside that loop or not. The result is shown in Figure 29. At each ring, the failure rate is obtained by taking the number of failed loops divided by the number of test units. For example, among the 60 test units, over 80% of the units have joint failure in loop 3. Much smaller failure rates were found for the most outside loops 1 and 2. Clearly, loops 3 and 4 show the most highest failure ratios. Since the die edge locates right between loop 3 and loop 4, this strongly implies that the local CTE mismatch (stress concentration) or local warpage plays an important role of initiating the failure. It should be noted that this phenomenon is seen for samples under both of the two temperature profiles. Also, this observation further demonstrates the DNP effect does not exist for this BT-substrate BGA.

5.4. Intermetallic Compound Effect

For all solder joints of TFBGA, it was found that a layer of intermetallic compound (IMC) formed near the interfaces of joint/substrate and joint/board. Energy dispersive X-ray analysis verified the IMC to be Au-Sn IMC. It is believed that, during reflow process, the Au plating on the substrate pads diffuses into the solder joints to form noodle-like AuSn₄ IMC (Figure 30) and later precipitates to near both interfaces of joint/substrate and joint/board during thermal cyclic process. Figure 31 shows the Au-Sn IMC formed near the interface of solder joint and substrate, while the Au-Sn IMC formed near the interface of solder joint and test board is shown in Figure 32. The thickness of the Au-Sn IMC is about 4µm to 5µm. Since Pb cannot react with Au, it gathers on the top of Au-Sn IMC (Figure 33) after Sn reacts with Au. As temperature cycling proceeds, the fatigue damage accumulates and the grain structure of the solder joint coarsens. At some point, microvoids or cavitations form at grain boundary intersections and eventually grow into microcracks. Cracks usually initiated from the edge of joints near the solder mask due to stress concentration and propagated along either the interface of the solder/Pb-rich phase or the interface of solder/Au-Sn IMC. Figure 33 shows a typical failure mode on the package side. It is clear that the existence of the interface of solder and Pb-rich phase could weaken the strength of solder joints. Thus, the formation of Au-Sn IMC should be avoided. To eliminate the effect of Au-Sn IMC, the thickness of Au plating on the substrate pads should be limited.

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Figure 28. Solder joints are divided into 6 loops.

Figure 30. Au-Sn IMC in the joints.
For Film BGA, the Au-Sn IMC seen previously in TFBGA is not observed in this case since the pad finish for Film BGA is either HASL or OSP. Instead of Au-Sn IMC, a new IMC Au-Sn-Cu (Figure 34) was formed between the substrate pad and the solder. Since the IMC is not Au-Sn, the failure mechanism is thus different. The failure is no longer along the interface of either solder/Pb-rich phase or solder/Au-Sn IMC. The crack was found to initiate from the corner of the solder ball and the polyimide and propagate into the solder (Figure 35). Attention should be focused to the fact that the failure interface is not along the Au-Sn-Cu IMC. It should also be noted that a study\textsuperscript{24} on Film BGA with Au/Ni finish does exhibit similar failure mechanism to the TFBGA. As for micro-BGA, the IMC formed is Au-Sn-Cu (Figure 36), which is also different from the case of TFBGA. The failure was again found to be inside the solder, not along the interface of the IMC and the solder. As for BCC and BCC++, since the Au plating thickness on the terminal is only 0.03 microns (compared to 0.5 microns on substrate pad of TFBGA), the quantity of Au is too little to form Au-Sn IMC. As a result, the failure of BCC family is all within solder (Figures 22 and 23).

Figure 31. Au-Sn IMC formed near the interface of joint and substrate (TFBGA).

Figure 32. Au-Sn IMC formed near the interface of joint and test board.

Figure 33. Cracks propagate along the interface of joint and test board (TFBGA).

Figure 34. Au-Sn-Cu IMC formed near the interface of joint and substrate (Film BGA).

Figure 35. Cracks do not propagate along the interface of Au-Sn-Cu IMC and solder (Film BGA).
6. Conclusions

The joint fatigue life of rigid BGA (PBGA and TFBGA), flex BGA (Film BGA), micro-BGA, and BCC/BCC++ is studied in this work. The effects of temperature profile, joint standoff, polyimide thickness, epoxy thickness, test board surface finish, and solder paste composition on the joint fatigue life are also investigated. The temperature ramp rate has significant effect on the joint fatigue life. Attention to the temperature ramp rate should be paid not to reach the level of thermal shock. The effect of joint standoff on the fatigue life can be well predicted by shear strain energy density in the solder joint. The effect of polyimide thickness on the joint fatigue life is found to be more significant than does the die paste thickness. The surface finish of test board also has influence on the joint fatigue life, although the difference in OSP and HASL is not significant. Further comparison with Au/Ni plating surface should be made. When a 2% of silver additive is added to the eutectic solder paste, the joint fatigue life is found improved.

The difference in pad configuration between the substrate and the test board is found to induce different levels of stress concentration and thus cause different levels of damage. This effect is the same for both rigid- and flex-BGA. The effect of chip size on the effective CTE is shown by Moiré fringe patterns. DNP effect is found to be very insignificant for either rigid- or flex-BGA in this study. However, the die edge effect is demonstrated to be very tremendous. This can be due to the stress concentration and warpage near the edges of chip caused by local CTE mismatch and the changes in flexural rigidity. Surface finish of test board affects the formation of IMC. For Au/Ni surface finish, the IMC is Au-Sn, while for OSP and HASL, the IMC is Au-Sn-Cu. Among them, Au-Sn IMC is found to degrade the joint fatigue life. The Au plating thickness on the substrate pads should be limited when an Au/Ni plating test board is used.

7. Future Work

The formation and effect of IMC on the fatigue life and failure mode need extra attention, especially when different surface finish and Au plating thickness are applied.

Acknowledgments

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About the authors

Sung-Ching Hung serves as a senior R&D engineer at ASE. He is in charge of designing and characterization of new packages. He received his B.S. Degree in Mechanical Engineering from National Sun Yat-Sun University (NS YSU) in Kaohsiung, Taiwan in 1987. In 1989, he entered the Graduate School of Auburn University and received his M.S. Degree from the Mechanical Engineering Department in 1991. Later, he entered the Graduate School of the University of Texas at Austin and received his Ph.D. from the Aerospace Engineering and Engineering Mechanics Department.

Po-Jen Zheng joined ASE in 1996 and serves as an Engineer in the fields of reliability and failure analysis. He received his B.S. Degree in Physics from Tung-hai University in Taichung in 1992. Then, he entered the Graduate school of NSYSU and received his M.S. Degree from the Material Science Department in 1994.

Hung-Nan Chen is currently a senior engineer in the R&D Lab of ASE and is responsible for thermal characterization of IC packages. He received his M.S. Degree from the Mechanical Engineering Department of Tatung Institute in 1993. In 1991, he was awarded a B.S. Degree from the Aeronautical Department of Tamkung University.

Shih-Chang Lee serves as a Project Engineer and is in charge of process development of new packages. He received his B.S. Degree in Mechanical Engineering from ASYSU in 1992. In 1993, he entered the Graduate School of National Cheng Kung University in Tainan and received his M.S. Degree from the Engineering Science Department in 1995.

J.J. Lee joined ASE in 1984 as an Engineer after graduating from the Aeronautical Department of Tamkung University. Since then he has been in the positions of Process Engineer, R&D Engineer, Engineering Supervisor, Manager and Director of R&D Engineering Department. Currently, he serves as the VP of the Engineering Department.