Synchronous DC/DC Converters in High-Current Processor Power Delivery Systems

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Abstract

Best performance of power delivery systems is detrimental to the successful operation of GHz range microprocessors. The location of the power sources in close proximity of the processor module has been possible due to improved packaging technologies. With the advances in MOSFET technologies, switching a DC/DC converter at several MHz has become rather common. Likewise, current capabilities of these switching power devices have been significantly enhanced. With this, simultaneous reduction in the size of the converters has been achieved while also achieving increased performance. Reduction in the ripple currents of basic DC/DC converters that are an integral part of voltage regulator modules (VRMs) has been attempted. Configuring several individual DC/DC converters in interleaved fashion has enabled researchers to handle the ripple currents through the VRM phase inductors. Also, multiple phases of these converters are required in order to meet the increasing transient power requirements of the load. In this paper, the application of a multiple-phase, full synchronous DC/DC converter when connected to a microprocessor power delivery system is addressed. Performance evaluation of the complete power delivery system based on a single and four-phase DC/DC converter is achieved. Advantages and disadvantages of each design are noted. Comparison is also made for various load representations. The load representations considered include a piecewise linear current source, and a first and second-order polynomial voltage controlled current source. Differences in the output characteristics with a simple DC source and its replacement with an actual VRM are also highlighted in this work. The contributions of the paper include setting guidelines in determining appropriate use of ideal or realistic power sources for power model analysis. The assessment of validity of these sources and their effects on the transient performance are key elements of this work. The paper is concluded providing thoughts on future directions.

Key words:
Processor Power Delivery, VRM, Decoupling Capacitors, and Voltage Regulation.

1. Introduction and Background

Voltage regulator modules (VRM) that are an integral part of the power processing stages beyond the silver box have undergone tremendous growth. These advances have been possible due to the technological advances in MOSFET and other device technologies, processes and improvements in their switching frequencies. The reduction in sizes of devices has also lead to several levels in the integration of control and power circuits. Several VRM topologies applicable for microprocessors have been studied. A buck converter with a synchronous rectifier has been the best candidate for the VRMs of microprocessor power.
supplies for a long time. Studies on topologies of synchronous buck converters fed from 12V is reported in Reference. Analysis when the VRM is fed from a 5V input is also available in Reference.

On the other hand, the operating voltage of microprocessor CPUs has constantly declined and may be below 1V in the near future. The current levels may exceed 100A at the output of a VRM. Of the noticeable breakthroughs in this direction is the rigorous need to enhance the switching frequencies of VRMs from the current few hundred’s of kHz to several MHz. Adopting more than one phase for conducting the increased currents is another recent approach. Increasing the number of phases drastically reduces VRM filter element sizes and reduces VRM response time. Due to multiple phases conducting over any cycle, the ripple current is also reduced at the output of the VRM. Studies relating performance while paralleling several VRM phases have been reported. Experimental work has predicted the efficiency attainable in these configurations. However, achieving these VRM efficiencies in the 90% range still remains a constant challenge.

Application of a switching power converter in the power supply scheme of a typical Microprocessor is the subject of this paper. A multi-phase VRM model and its design considerations are given in Section 3. Power model performance when fed with a simple voltage source and an actual four-phase switching VRM is discussed in Section IV. Comparison is made of the effect of different die load representations. Also, responses of a single-phase VRM and a four-phase VRM are studied. The input voltage of 12 V is chosen in the analysis.

2. Lumped Model of A Processor Power Delivery System

Figure 1 represents the lumped power model of a typical microprocessor. The various loops represent stages of package and interconnect. The model elements actually are interconnect element parameters and their parasitics. The first and second level of decoupling is provided by the capacitors Cpkg and Cint. The die can be represented in several ways. A voltage controlled current source representation G is shown in this case. The battery in series with an inductor and a capacitor across the combination serves as a simple source to the power model. A switching power supply marked ‘Powerpod’ in Figure 1 replaces this simple source when the case is that of a realistic switching power source. The integral component of the switching supply is the voltage regulator module (VRM). The VRM attaches to the rest of the power delivery system via a connector. The processor voltage Vcc is monitored across the nodes 3 and 2 as shown. The die voltage across nodes 6 and 7 is monitored to determine if the circuit meets transient droop voltage specifications. The circuit model when fed with a simple source is passive, whereas, with the VRM as the input stage, the circuit becomes an active circuit that involves feedback control (voltage across points marked ‘volt-

3. VRM Model

Figure 2 (a) represents the equivalent circuit of a buck type VRM model. The main switch S1 enables the step down of the input voltage. L and Cc constitute the low pass output filter elements. The duty ratio D of the converter is the ratio of the input voltage Vin and the output voltage V0. Switch S2 conducts at all other times when the main switch S1 is off. Thus, the current Ic in the inductor L varies between values of Imin and Imax as shown in Figure 2(b). The two switches are switched at a rate that is termed as the VRM switching frequency fs. The switch S1 can be a fast diode or a MOSFET. When the switch S2 consists of a MOSFET instead of a diode, the configuration represents a synchronous rectifier topology. Eref is the voltage whose value is to be maintained across the monitor points as Vcc. It serves as one of the inputs to a comparator inside the controller that implements both VRM voltage and current feedback.

Figure 2(a). Schematic of a synchronous-rectifier based buck converter.
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3.1. Multi-Phase VRM

Figure 3 shows the block diagram of a four-phase VRM without the control and driver circuitry. The advantages of multi-phase VRMs were mentioned earlier in terms of reduced cost, size and improved response time. A multi-phase VRM consists of several phases in which each phase conducts for an equal part of each cycle. Within each phase, the two switches conduct in the same manner as described in the basic converter. Each phase consists of a per-phase inductor. However, a single bank of bulk capacitors is used at the output point where all the phases combine.

3.2. VRM Design Considerations

The magnitude of the current that a VRM has to supply also determines its transient requirement. The initial rate of application of the load current is effectively met by the interconnect and package stages. The minimum theoretical response time of the VRM is given by Equation (2), of the form,

$$ t_{response} = \frac{\Delta I \cdot L_f}{\Delta V} $$

where $\Delta I$ is the change in converter output current, $\Delta V$ is the change in the voltage across the inductor and $L_f$ is the inductor value. As an example, if $V_i=12V$, $V_o=1.5V$, and the current in a 50nH inductor varies between 50A and 75A, then $\Delta V=12-1.5=10.5V$, $\Delta I=75-50=25A$. The theoretical response time of the VRM in such a case is 120ns.

4. Simulation Results

Extensive simulations are done to study the power model performance. The simulations are carried out on Orcad Pspice A/D. First, a study with the power model when fed with a simple voltage source is presented. Then, the droop study is repeated with the complex VRM model replacing the simple VRM. Comparison is made of the data when a single-phase and a four-phase
VRM supply the circuit. Different die load representations are also studied.

4.1. Comparison of Simple and Actual VRM Models:

A simple VRM model consists of an ideal battery in series with a small resistance and an inductance and a bulk capacitor across the combination. A transient current load is applied at the die in order to study the voltage droop characteristics. The waveform of the voltage \( v_{dc} \) across the die of Figure 1 for both the simple source and a four-phase VRM as sources is illustrated in the bottom traces of Figure 4(a). The top trace is of the voltage \( V_g \) measured after the power POD connector in Figure 1. The voltage droop target for both cases is 10% below \( V_{cc} \). Three distinct droops are expected in the waveforms corresponding to the package-die, interposer-package, and VRM-interposer loops. In the waveforms that pertain to the complex VRM case, the VRM feedback control loop responds and the voltage begins to rise to the required \( V_g \) value after the third droop. Whereas in the simple source case, the voltage continuously decreases as there is no control and hence a third droop is not seen. The first droop voltages are 1.133V and 1.130V, the second droop voltages are 1.164V and 1.163V, and third droop voltage for the case with VRM is 1.158V. This means that for the first and second voltage droops, no significant difference between using a simple VRM model and a four-phase VRM. A comparison of the transient response of the VRM that feeds the power model of Figure 1 is illustrated in Figure 4(b), where the current supplied at the die and the current in the connector which is the sum of all VRM phase currents are shown. The current drawn from a simple VRM is comparatively lower than that drawn from a four-phase VRM model due to large amounts of bulk capacitors used in the simple VRM case.

4.2. Comparison with Single and Four-Phase VRM Models as Sources

A 250kHz single-phase and 1MHz/ph, four-phase VRMs, whose design values were provided in Table 1, were tied as inputs to the lumped power model. The waveforms of the voltages across the die and after the power POD connector are shown in Figure 5(a). The currents at the output of the VRM and at the die are shown in Figure 5(b). As can be observed, the response time of the four-phase model is much smaller than that of the single-phase model due to its much smaller inductance per phase and the much lesser bulk capacitance. A similar observation can be made on the current response. The single-phase VRM provides a slow and flat transient response to the load than the four-phase VRM. In other words, VRM switching frequency and the number of VRM phases do determine the response characteristics of the VRM. Also, a comparison of the droop voltages obtainable in the four and single-phase cases, in addition to that with a simple VRM are shown in Table 2 in which the ideal case entries are from the previous section. From the second droop data in Table 2, one can observe that the slower single-phase VRM design is not as effective as the faster four-phase VRM design for this power delivery system. This comparison also signifies currently achieved industry VRM frequencies.
4.3. Comparison with Different Die Load Representations

The effect of different die representations is investigated when the lumped model was fed with an actual VRM. The droop voltage values and obtained currents at the die and at the edge connector with a single and double order voltage controlled current source G representation of the die and with an ideal piecewise linear current source \( I_{pw1} \) are represented in Figure 6. The voltage across the die nodes 6 and 7 and a piecewise linear voltage source across nodes 10 and 0 constitute the elements of the second order polynomial G source. As can be observed from the droop waveforms, the difference between a single-order polynomial and the piecewise linear case is not great as compared to the double-order polynomial case. It can be concluded that a piecewise linear representation predicts more pessimistic droops than the other two as the current achieved from a piecewise linear representation is comparatively higher than that achieved from the other two representations.

Table 2. Effect of single and four-phase designs on droop characteristics.

<table>
<thead>
<tr>
<th>Case</th>
<th>Droop1 (V)</th>
<th>Droop2 (V)</th>
<th>Droop3 (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal voltage source</td>
<td>1.133V</td>
<td>1.164V</td>
<td>NA</td>
</tr>
<tr>
<td>Single-phase VRM</td>
<td>1.130V</td>
<td>1.158V</td>
<td>1.154V</td>
</tr>
<tr>
<td>Four-phase VRM</td>
<td>1.130V</td>
<td>1.163V</td>
<td>1.158V</td>
</tr>
</tbody>
</table>

5. Conclusion and Future Directions

Application of a synchronous rectifier type of buck converter in a typical microprocessor has been discussed in this publication. A lumped power model of the processor is considered in the study. A simple VRM and a four-phase complex VRM as sources and their transient responses are compared. The simulations yield no significant difference in the first and second voltage droops when using a simple and a four-phase VRM. With an actual VRM, due to the voltage feedback, the voltage begins to rise towards \( V_{cc} \) value after the third droop. Whereas with a simple VRM, it continuously decreases as there is no control, and hence, a third droop is not seen. The current drawn from a simple VRM is comparatively lower than that from a four-phase VRM model due to the large bulk capacitance used. A single-phase VRM provides a slow and flat transient response to the load than the four-phase VRM. Also, a comparison of the second droop voltages indicates that a 250kHz single-phase VRM design is not as effective as the 1MHz/phase four-phase VRM design for this power delivery system. As far as different die representations, a double polynomial representation is close to a real system than a piecewise linear or a single-order polynomial load representation since it takes the actual voltage available at the die into consideration than the other two in driving the load current. Hence, a piecewise linear representation predicts the most pessimistic droop of the three as it draws the highest current, a current which is not realistic.

The outcome of this work is that for first and second droop analysis analysts can use a simple VRM so that results can be obtained instantaneously. However, if the effect of power supply is in perspective, the analysis must include the VRM and its feedback control loop behavior. These distinctions are very essential in conducting sensitivity simulations and also to have an actual idea of the times required for analysis. Also, the studies can serve in identifying bottlenecks in the model stages. As a future direction, comparison between lumped and distributed model performances will be attempted so that similar guideline can be established for future simulation and analysis. Improved techniques for prediction of accurate lumped models from distributed package and interconnect power models will be attempted in parallel.

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