Ultra-Fine Photoresist Image Formation for Next Generation High-Density PWB Substrate

Fuhan Liu*, Venky Sundaram, George White, and Rao R. Tummala
Packaging Research Center
Georgia Institute of Technology
813 Ferst Drive
Atlanta, Georgia 30332
Phone: 404-385-0731, 404-894-9394, 404-894-0514, and 404-894-9097
Fax: 404-894-3842
e-mail: fliu@ee.gatech.edu, vsunda@ee.gatech.edu, georgew@ee.gatech.edu, and rao.tummala@ee.gatech.edu
* Visiting Scholar, Fudan University, Shanghai, China

Abstract

System-on-a-Package (SOP) is fast becoming a primary key towards the drive for integration of mixed technologies such as RF, digital, analog, MEMS, and optical at the electronic package level. A key enabler of this technology is a fully integrated substrate, called Single Level Integrated Module (SLIM), with very high wiring density and integrated passive and optoelectronic components. This paper presents an overview of the SLIM testbed integration process and test vehicles, with particular emphasis on ultra-fine resist lithography and microvia processing. This paper will focus on the issues, challenges, and results for achieving very fine line and ultra fine line image formation on fiber glass reinforced epoxy substrates for next generation electronic packages. Four commercial photoresist materials were evaluated for their imaging resolution. The exposure and development processes have been optimized and several related effects, which limit the fine line imaging, have been investigated. Line widths down to 7.5 µm have been achieved at the Packaging Research Center (PRC) on PWB substrates using low cost liquid photoresist and associated processes over a large area.

Key words:

SOP, SLIM, Fine Line, High-Density Wiring (HDW), Photore sist, Dry Film, and PWB.

1. Introduction

Electronics is one of the world’s largest industries, accounting for almost 1 Trillion dollars worldwide. The single most important and fundamental technology fueling this industry is that of semiconductor microelectronics. This technology has revolutionized every aspect of electronic products in automotive, consumer, computer, telecommunications, aerospace, military, and medical segments by ever higher integration of transistors (20 million per chip) at ever continued lower cost per transistor during the last four decades. This integration and cost path has led the industry to believe in so-called system on-a chip (SOC) for all application areas and products.

The Packaging Research Center (PRC) believes that SOC is not the ultimate solution for all applications, especially beyond the year 2007, and has proposed a fundamentally new paradigm called System on-a Package (SOP)\(^1\). SOP aims to address the technical, legal, and financial problems anticipated with the SOC approach for next generation electronic products. The technical problems relate to the mixed-signal requirements of future products, mixed technology systems, design issues, and limitations of on-chip performance that the industry faces for the first time. The financial problems are to do with the cost of large IC, and the slowdown in the reduction of cost per transistor as a result of very low IC yields, and very high wafer fab costs that are estimated to be in 3-5 Billion Dollars. The legal problems arise due to the requirement for integration of intellectual property from...
multiple, possibly independent sources, with attendant interoperability, integration, and liability hurdles. SOP is expected to offer an advantage in all these areas. The SOP strategy will include benchmarking SOC and SOP technologies for two classes of systems that are expected to dominate the internet-driven world of the 21st century: (a) wireless base stations and handsets, and (b) high performance multiprocessor servers.

At the heart of the new SOP strategy is a fully integrated single level integrated module (SLIM) substrate with ultra-high density wiring and integrated passive and optoelectronic components. The two major goals of the substrate technology are highest level of integration incorporating added functionality to the substrate; and lowest cost. The PRC is developing novel technologies for low-cost, integrated substrates involving multilayer thin films using sequential build-up (SBU) technology on organic laminates.

2. High Density Wiring Technology Need

One of the primary building blocks of SOP/SLIM technology is ultra-high density wiring on low-cost substrates. The latest IC packaging roadmaps published by various organizations like NEMI, SIA predict the need for 10-15µm substrate wiring and microvias in the next few years to meet the high I/O density requirements of next generation ICs. There is an ever-widening gap between the needs for IC packaging and the capabilities of the PWB industry as illustrated in Figure 1.

![Figure 1. PWB manufacturing technology gap.](image1)

Figure 1. PWB manufacturing technology gap.

Significant progress has been made in line width capability in Printed Wiring Boards since 1995 with 75-100µm fine lines currently being used in production. Furthermore, new microvia substrate technologies are attempting to bridge this gap using novel enhancements to the interconnect density in substrates. The current state-of-the-art microvia technologies worldwide involve 30-40µm line widths and spaces and 75-100µm microvias. The future trend in high-density boards and the various technologies in practice are shown in Figure 2.

![Figure 2. Microvia board roadmap indicating PWB needs for different IC generations.](image2)

As illustrated in this roadmap, the PRC is exploring ultra-high density wiring in the 15-25µm range with 25-50µm microvias. This is expected to transition to 6-10µm line widths and spaces and 10-15µm microvias in the next few years. The current process integration research at PRC is based on low-cost epoxy-based dielectrics, photo and laser lithography, and low-cost, plated metallurgies, all developed on low-cost FR-4 substrates. Recognizing the need for CTE matched low-cost substrate platforms for future SOP needs, the base substrate program at the PRC is exploring novel alternate substrate materials that could potentially lead to the elimination of underfill in Flip Chip processes and also more environmentally friendly materials like halogen-free boards. This paper presents an overview of the SLIM testbed integration process and test vehicles, with particular emphasis on ultra-fine resist lithography and microvia processing.

3. SLIM Testbed and Process Flow

The current generation of SLIM test vehicle involves high density wiring layers, integral passive components, Flip Chip assembly with underfill, and novel design methodologies. This test vehicle, named SLIM-2B, will serve as a tool for substrate build and assembly process demonstration and characterization, yield analysis, validation of models for passives and design, optical interconnects, and thermal module attachment.

SLIM-2B test vehicle consists of a rigid 300mm x 300mm FR-4 substrate. A sequential build-up process is used to add up to three high density wiring layers with microvia interconnects. Thin film capacitor, resistor, and inductor layers are also fabri-
cated using materials and processes compatible with the rest of the test vehicle. The design ground rules for the SLIM-2B test vehicle consist of 25µm line widths and 50µm spaces between lines. The smallest microvia diameter is 50µm. The thickness of the interlayer dielectric is 25µm, and the copper metal thickness is typically 8-10µm. The thickness of the capacitor layer is between 6 and 10µm and the minimum geometry for the capacitor is 100µm (4mil) square. The resistor thickness is around 15µm, and the geometry of the resistors is similar to that of the capacitors. The materials set used in the current SLIM-2B test vehicle is listed in Table 1.

Table 1. Materials used in SLIM-2B test vehicle.

| · Substrate – High Tg FR-406 laminate, 1mm thick, 1/4oz Cu foil (9µm thick), 300mmx300mm, |
| · Dielectric - Dupont ViaLux 81™ dry film epoxy, 25µm (1mil) thickness, |
| · Conductor – Copper, treated foil on base layer, electroplated Cu on other layers, |
| · Photoresist - Dupont Riston dry film negative resist, 15µm (0.6mil) thick, |
| · Capacitor - PMN-PT or BaTiO₃ filled epoxy (Ciba LMB7081), 45-55 volume% fillers, |
| · Resistor - Carbon filled epoxy paste, |
| · Inductor - Copper (2D and 3D), and |
| · Soldermask – Ciba Probimer 65M or 77 liquid photoimageable soldermask. |

The process flow for SLIM-2B consists of double-sided build-up of alternate thin copper and dielectric layers, with embedded capacitor, resistor, and inductor layers. The first layer circuit traces are defined by a subtractive etch process using an alkaline spray etch process (ammonium persulfate based chemistry). The dielectric dry film epoxy is then vacuum laminated on the substrate. This process results in excellent planarization over the underlying circuitry as illustrated in the results section. Microvias down to 50µm diameter are created in the photoimageable epoxy using a UV exposure process through a mylar phototool held in intimate contact with the substrate, followed by heat treatment and developing in gamma butyro-lactone (GBL). The vias and the dielectric surface are passed through a standard permanganate based roughening process followed by seed electroless copper plating. The copper traces are built-up through a dry film photoresist using pattern electrolytic plating using an acid copper chemistry. Finally, the photoresist is stripped and the seed copper layer is etched back using a mild microetch chemistry. This completes the metallization process and the next dielectric layer can be added and the process repeated to form a multilayer stack-up.

4. ITRI HDI Fine Line Test Vehicle

The PRC prototype team was the only university group to participate in a study by the Interconnect Technology Research Institute (ITRI) to evaluate the fine line capabilities of US high density substrate fabricators (HDI Fine Line Project, Phase I). This test vehicle is a process capability panel designed to provide specific information about manufacturing capability and quality. The board design consists of a double sided core, approximately 0.7mm (28mil) dielectric with 1/2 oz. over 1/2 oz. Cu weight each side. It has one high density build-up layer on each side with a 40+µm dielectric thickness. Board size is 266mm (10.5") x 184mm (7.25") and contains 60, 25mm x 25mm coupons of five designs evaluating conductor formation, via formation (buildup to core layer), and registration (buildup to core layer). The process flow and materials set for this test vehicle was similar to that of the SLIM-2B test vehicle described above. The following sections describe some of the results from SLIM-2B and ITRI test vehicles and discuss the various factors that influence fine line lithography on PWB substrates.

5. Results and Discussion

The first set of conductor test coupons on the ITRI test vehicle consisted of 25, 50, 75, and 100µm lines with 50, 75, 100, and 125µm spaces. All of these features were successfully imaged using dry film resist and plated using pattern plating. Figure 3a shows the plated copper lines down to 25µm. The second set of conductor patterns included isolated fine lines of 25-100µm widths with large spacings. The third test coupon was designed to test the capability to open narrow spaces between very thick lines or features. Successfully imaged and plated test structures of this type are shown in Figure 3b. Microvias down to 25µm have also been successfully imaged and opened in photodielectric dry film (PDDF). The vias are metallized with electroless flash plating and pattern electroplating to form the interconnect. Figure 4 shows a cross-section of a plated 50µm (2mil) microvia from the SLIM-2B test vehicle.

Figure 3a and 3b. Fine line conductor patterns from ITRI HDI fine line test vehicle.
Sufficient plating thickness on the via wall, such as shown in Figure 4, is necessary for reliable interconnection. The use of dry film epoxy has some advantages over liquid epoxy dielectrics. The handling and processing of the dry film is simpler and the cover sheet on the film protects it from dust during deposition and lithography. Due to the pressure applied to the epoxy during lamination, the planarization achieved over the underlying circuitry is better with dry film epoxy, as seen in the cross-section.

Figure 4. Cross-section of 50µm microvias from SLIM-2B test vehicle fabricated in PDDF.

6. Ultra-Fine Resist Imaging and Lithography

One of the key issues in achieving ultra-high density wiring is the primary imaging and circuit patterning process. The current options include stencil printing of conductive ink, photolithography of liquid or dry film resists, and laser direct imaging. The majority of current primary imaging done in the industry today involves photolithographic processing. This study used UV lithography on liquid and dry film negative photoresists. Different surface finishes encountered in typical PWB and HDI processes, including untreated copper foil with microetch or plasma roughening treatments, double-treat copper foil, and electroless plated copper were used.

The two liquid resists were deposited by spin coating or meniscus coating. The PRC has already demonstrated highly uniform coatings with <1 volume% material wastage using meniscus coating 6. The dry film resists, C1 (15mm thick) and C2 (37.5 mm thick) were laminated on the substrate using a Dupont SMVL-100 vacuum laminator. Both soft and hard photomasks were employed in this study. 350mm (14”) x 350mm (14”) mylar phototools (halide on polyester) were plotted at 1.6µm (1/16mil) resolution and chrome-on-glass masks (150mm x 150mm) were also fabricated for geometries less than 20µm. The mylar masks are limited by current plotter resolutions of about 20 µm. They are also prone to wear and thermal expansion. The glass masks provide improved resolution, dimensional stability, and durability, but are more expensive 7.

A Tamarack 152R contact printer with a 1kW UV source was used for the exposures. This tool provides the benefits of collimated UV light, which is essential for fine line lithography. Vacuum hard contact was used for all resists and photomasks. The resists were spray developed and the entire process was performed in a class M4.5/1000 cleanroom. A 2D Design of Experiments (DoE) matrix was used for optimizing the exposure dose and development parameters.

The dry film resist images down to 25µm were illustrated in Figure 3 earlier. Line widths of 10µm were successfully developed using the low cost liquid photoresist B, as shown in Figure 5a. The finest image achieved was 7.5µm using liquid photoresist A, with good edge definition, as shown in Figure 5b. The typical results achieved using dry film and liquid photo-resist are summarized in Table 2.

Figure 5a. Micrograph of 10µm conductor lines and spaces in low cost liquid resist B.

Figure 5b. 7.5µm lines imaged in liquid resist A.

Table 2. Summary of imaging results for four commercial photoresists.

<table>
<thead>
<tr>
<th>Type</th>
<th>Liquid A</th>
<th>Liquid B</th>
<th>Dry film C1</th>
<th>Dry film C2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acting Coating</td>
<td>Negative</td>
<td>Negative</td>
<td>Negative</td>
<td>Negative</td>
</tr>
<tr>
<td>Thickness, µm</td>
<td>Spin</td>
<td>Spin</td>
<td>Vacuum Lamination</td>
<td>Vacuum Lamination</td>
</tr>
<tr>
<td>Cost</td>
<td>Meniscus</td>
<td>Meniscus</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>Line/Space, µm</td>
<td>7.5/7.5</td>
<td>10/10</td>
<td>25/25</td>
<td>50/50</td>
</tr>
</tbody>
</table>
7. Factors Affecting Fine Line Lithography

UV Exposure: Precise control of the UV exposure dose is critical to fine line lithography. Since the UV exposure progresses from the resist surface to the bottom, under-exposed resist will swell and/or lift off during the subsequent development process due to insufficient cross-linking at the bottom of the film. Extreme overdose during exposure can result in incomplete development and resist residue in the developed areas. Over exposure can also lead to unwanted effects like heating, scattering, and reflection. Dry film resists are easier and safer to handle than liquid resists, but cannot reach the higher resolutions possible with thin liquid resists. Mylar cover sheets on dry film resists protect the surface from contamination but could reduce the resolution by preventing good photomask-to-resist contact.

Effect of Resist Thickness and Planarity: In theory, the image resolution is better for thinner resist films. However, planarity of the resist surface and thickness uniformity over large areas is also critical. In contrast to the extremely smooth surface of a semiconductor wafer, a FR-4 laminate has a rather rough and undulating surface. When resist is coated on this rough surface, thickness variations over the large panel are significant. Since the optimum UV exposure dose is highly dependent on the resist thickness, it is difficult to control the exposure uniformity across the entire substrate. For the copper-clad FR-4 used in this study, the height differential (Δh) was about ±1.5µm, and resists with thickness greater than 10µm were used to alleviate this effect.

Light Reflection and Edge Effect: Another effect observed was a very thin layer of residual resist along with the side walls on the bottom of the openings that looked like “frills”. This very thin residue was rather difficult to wash off with the developer. This phenomenon could be from the UV light reflections from the copper surface below the resist. Since the copper surface is quite rough, there is considerable amount of randomly oriented UV reflections that result in exposure and cross-linking of the resist in unwanted areas. This “frill” effect resulted in smaller openings and jagged edges on the resist and limits the fine line capability of the process. Careful control of the UV exposure dose might help to minimize this effect.

Adhesion: Photoresist adhesion to the underlying surface is an important issue for fine-line technology. Figure 6(a) shows a deformed fine-line comb pattern after development indicating insufficient resist to substrate adhesion. Experiment found that the resist etching rate was a function of the width of opening in the development process. When the openings became finer, the etching rate reduced, and the developing time increased. This results in attack of finer resist geometries (20µm), as seen in Figure 6(a) while wider resist patterns (50µm) were stable, as shown in Figure 6(b). These two comb patterns were located on the same board within a distance of only 1.5cm. Enhancing the adhesion between the resist and the underlying copper becomes more important for fine-line formation and needs more attention. Liquid resists tend to have better adhesion than dry films and surface treatment of the copper can be used to further enhance the adhesion.

8. Summary and Future Outlook

System-on-a-Package (SOP) technology aims at an integrated systems packaging solution for low cost, high performance, mixed signal systems for next generation consumer, computer, telecom, and automotive electronic products, with a silicon packaging efficiency of 80%. A key aspect of SOP/SLIM packaging is ultrahigh density wiring on low cost, organic substrates. The PRC team has demonstrated novel process integration testbeds including SLIM-2B and ITRI HDI fine line prototypes, with line widths and microvias down to 25µm, on large 300mmx300mm FR-4 substrates.
The resolution capabilities of four commercial photoresists on FR-4, process optimization, and some related effects that limit the fine line formation have been investigated. A pitch of 20µm (10µm line/space) has been demonstrated on low cost FR-4 laminates at the PRC using a low cost liquid photoresist. Extremely fine 7.5µm photoresist imaging on rigid organic substrates was achieved by using a negative photoresist. Dry film resists have been used to obtain 25µm line width and space.

To meet the long-term roadmap goals of 6µm lithography, liquid resists combined with thin film technology appears to be a potential solution, but significant developmental work and enhancements in other areas such as substrate materials, plating, and etching processes are necessary. Once developed, the ultra-high density wiring substrates will be integrated with embedded passives and optoelectronics, and utilized in conjunction with several other PRC technologies including Flip Chip assembly, optical devices, and thermal modules based on microjet cooling to develop next generation SOP prototypes.

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References


About the authors

Fuhuan Liu is a Visiting Fellow of the Packaging Research Center at Georgia Institute of Technology. He was an Associate Professor of the Department of Materials Science and Deputy Director of High Density Electronic Packaging Laboratory at Fudan University. He had been on a Research and Education Visit to Brandeis University from 1987 to 1988, and Visiting Scholar at Wayne State University and IMAPS from 1997 to 1998. Currently, his interests focus on the research and development of fabrication of System-On-a-Package (SOP)-the next generation package, Ultra-HDI with ultra-fine line and microvia technologies for high-pin BGA and CSP and fine-pitch Flip Chip, and integral passives. He graduated from Fudan University in China in 1965, majoring in Electron Physics. He has worked in various areas including Laser, Electronic Optics, Medical Physics, Metrology, Materials Characterization, Applied Physics, and Materials Science. He has received numerous professional national level awards in China. He is a member of IMAPS.

Venky Sundaram received his M.S. Degree in Ceramic Engineering from the Georgia Institute of Technology. Since 1997, he has been working for the Packaging Research Center as a Research Engineer responsible for process integration and development for next generation electronic packaging technologies. His primary focus has been on thin film process development on organic substrates and integration of thin and thick film passive components into high-density multilayer substrates. He has several publications in the packaging area and presented short courses on “Embedded Passives” at Nepcon West 1999, and Georgia Tech, June 1999, and a short course on “High Density PWB Technologies” at EMIT2000 in Bangalore, India.
George White is currently the Associate Director for Research of the Packaging Research Center at the Georgia Institute of Technology in Atlanta. Prior to joining the Packaging Research Center in November of 1998, he was employed by the Motorola Corporation of Schaumburg, Illinois. In this role, he managed the Government Programs Manager for the Applied Simulation and Modeling Research Group of the Corporate Computer Software Center. There, he served as program manager for the Motorola-led embedded mass formed passives consortium, the demonstration of electrical and mechanical design of low cost mixed mode modules and the holographic optical interconnect technology consortium. Prior to joining Motorola, he was employed at the International Business Machines Corporation, as a Development Manager for the Advanced Thin Films Group in Fishkill, New York. There, he developed low cost thin film processes for electronic packaging for IBM’s mainframe and cost performance products. He holds over 11 US patents, and a number of publications. He received his Ph.D. and M.S. Degrees from the University of Illinois in Metallurgical Engineering in Urbana, Illinois, and his Bachelor’s Degree in Physics from Hampton University in Hampton, Virginia.

Dr. Tummala is currently an Endowed Chair Professor in Electrical and Computer Engineering and Materials Science and Engineering at Georgia Tech. He is also the Director of the Packaging Research Center funded by NSF (as one of its Engineering Research Centers), the State of Georgia, and the U.S. electronics industry. Prior to joining Georgia Tech, he was an IBM Fellow at IBM Corporation, where he invented a number of major technologies for IBM’s products for displaying, printing, magnetic storage, and the industry’s first multichip packaging for which he received 16 technical, outstanding and corporate awards from IBM.

Dr. Tummala is a Fellow of both the IEEE and the American Ceramic Society, a member of the National Academy of Engineering, 1996 President and current International Vice President of IMAPS, and a Technical Vice President and a member of the Board of Governors for IEEE-CPMT. He was recently named by “Industry Week” as one of the 50 stars in the U.S. for improving U.S. competitiveness. He is co-editor of the widely used Microelectronics Packaging Handbooks.

He has published 160 technical papers and holds 66 U.S. patents and inventions. He has received a number of awards including the David Sarnoff Award, and sustained the Technical Achievement Award from IEEE, John Wagnon’s Award from IMAPS, Materials Engineering Achievement Award from ASM-I, both the Arthur Friedberg Memorial and the John Jeppson Awards from American Ceramic Society, the Total Excellence in Electronics Manufacturing (TEEM) Award from the Society of Manufacturing Engineers, and the European Materials Award from DVM. Dr. Tummala has received many academic and educational awards including Distinguished Alumni Award from the University of Illinois and the Indian Institute of Science in Bangalore. Most recently, he received the highest faculty award at Georgia Tech and gave a commencement speech in September of 1998. Dr. Tummala received his B.E. Degree in Metallurgical Engineering from the Indian Institute of Science, Bangalore, India, and his Ph.D. Degree in Materials Science and Engineering from the University of Illinois.