High Density Modular Packaging for Space Electronics

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Abstract

If miniaturization and reliability remain fundamental requirements for the design of Space electronic equipment, the economical aspects also drive more this specific domain of industry. Electronic packaging is currently being considered as an outstanding factor of competitiveness. Astrium, a major Space system and equipment manufacturer in Europe, developed a complete set of processes in order to cope with three objectives:

• smaller: use of MCM, 3D assembly, Grid Array SMD packages, high density PCBs,
• smarter: more complex functions, higher electrical and thermal performances, high reliability for Space environment, and
• cheaper: standardization, flexibility, reworkability, testability, high yield automated manufacturing, adaptability to next generation of components (non-hermetic technologies), and shorter time-to-market.

The best answer to this long list of issues is closely linked to High Density Interconnect use, at all packaging levels. MCM Very Fine Line substrates developed by Astrium are the first tile of this structure. They are followed by High density MCM packaging, ruggedizing, 3D interposers, specific cooling methods, and modular approach. This concept allows dismountable highly tolerant electrical, mechanical, and thermal assemblies of the different functions inside electronic units, applied to flight computers and processors for Space projects presently in development for French and European Space Agencies and for commercial telecommunication spacecrafts.

The present paper describes how MCM packages and BGA components are assembled on high density microvia PCBs and how they are cooled. A modular approach has been chosen, based on the use of “interposing contact arrays”, between microelectronic modules (that can be stacked) and boards, and between boards together (daughter and mother). These connectors, developed by Astrium, have a unique feature, nearly 1 mm stroke capability. They are available off the shelf or customized. They have been successfully submitted to a comprehensive set of space qualification tests. The paper will demonstrate also how a pseudo-hermetic encapsulation is used rather than expensive hermetic MCM packages. Due to the attributes of this ruggedizing method, cost is reduced and hermetic feature is maintained.

Key words:

Space Equipment, Electronic Packaging, 3D, Connector, Interposer, Interconnection, Modularity, Ruggedizing, and MCM.
1. Introduction

Due to their high number of external connections, most of the available standard packages for MCMs are now QFPs in SMT mode. But, the increasingly pins number of such functions leads to the recent development of BGA type packages, most of these packages being custom manufactured. Nevertheless, such large packages, having soldered fine pitch or blind connections, present a lot of difficulties, both at the assembly and the reliability levels.

The requirements for the highly reliable connections that are needed in Space applications for digital equipment, can be summarized as follows,
• High density and high packaging efficiency,
• Easy testability of MCM packages,
• Easily Dematable connections,
• High compliance with large thermal variations,
• Large assembly margin,
• High power dissipation capability, and
• Modularity.

The researchers’ experience shows that the Achilles’ heel of high density electronics is the interconnection at all intermediate packaging levels, therefore, with high complexity functions as MCMs, it is often required to remove the package in order to either test it or replace dice inside it. In this case, an intermediate socket is preferable to a dangerous desoldering process.

The researchers present hereafter a global solution to high-density modular packaging starting from MCM substrates up to the equipment assembly, this study having been co-funded by the French CNES Agency.

2. 3D High Density Modular Packaging Concept

In order to fit to new telecommunication payload requirements, Astrium has developed a new modular Space equipment architecture presenting both a very high packaging efficiency and a high thermal dissipation capability. This concept is based on several original features,
• Very Fine Line, mineral, MCM solution,
• New LGA, single or dual sided, hermetic or ruggedized, MCM packaging concept,
• 3D assembly concept, permitting up to six dice levels per PCB area,
• Dematable concept, based on interposers, at MCM levels and between mother and daughter PCBs, and
• Efficient materials and thermal parts, for power extraction from MCMs.

Figure 1 shows the high-density modular architecture, which presents both a direct thermal path between the MCMs and the mechanical structure, and a tolerant electrical link between the daughter board and the mother board. Indeed, the deal for a power dissipating equipment is induced by the fact that it is not possible to have both a high pressure to a thermal spreader located on the lower structure and the precise adjustment of each daughter board to rigid connectors mounted on the mother board. Moreover, due to this original solution, conventional components such like QFPs can also be soldered under MCMs, increasing the global packaging efficiency.

3. MCM-VFL

Substrates with high density interconnect are the key component for the manufacture of MCMs. Astrium technology is named “VFL” for Very Fine Line. It is an evolution of conventional thick film hybrid process for which Astrium received a Space qualification in 1983. This process is characterized by three main features;
• Mineral layers deposition by screen printing,
• Lines and gaps definition, by photolithography, and etching process (as for thin films), and
• Vias drilling by Excimer laser.

The main characteristics obtained in this case are as follows;
• Lines and gaps width: 100 to 38 µm, with an actual lower limit at 25 µm,
• Gold conductor thickness: 8 µm,
• Conductor resistivity: 10 mΩ/sq. max,
• Low K (4.5 typ.) dielectric thickness: 25 µm,
• Vias diameter: 100 to 38 µm, with an actual lower limit at 25 µm,
• Vias resistance: < 50 mΩ,
High Density Modular Packaging for Space Electronics

- Number of metal layers: up to 5,
- Substrate size: 90 mm × 90 mm max. Currently, Alumina, AlN in progress,
- Buried capacitors: 20 nF/cm², and
- Buried resistors: in progress.

Figure 2 shows a DSP application on a 64 mm × 46 mm substrate, with four conductor levels, 22 meters of total track length and 3700 vias.

4. LGA - MCM Packaging

MCMs for spaceborne applications are based on high temperature cofired ceramic packages technology. The current of MCMs is single sided hermetic cavity with sealed rings and welded metal lids. This technology is primarily chosen for its high reliability, mechanical strength, thermal performance and for its compatibility with materials, assembly processes and performance specifications in case of Space qualified microcircuits. The interconnection of such packages is stated in two main families: Quad flat pack Kovar peripheral leads (QFP), and Grid Arrays in both Ball Grid Array (BGA) and Land Grid Array (LGA) configurations.

Until recently, the growth of MCM package I/Os number has led to their lead pitch reduction, and also to the increase of their size (see Figure 3). Due to reliability, manufacturing and assembly process difficulties, this pitch is limited to 0.3 mm. A pitch of 0.635 mm to 0.5 mm is widely used for hermetic MCM packages whilst their overall dimension is reasonably limited to 100 mm × 100 mm and the number of leads to 600. Compared to the 300 to 500 I/Os generally needed by processor functions, this number seems to be sufficient. But, the main drawback of MCM packages with peripheral leads is the risk to damage them during test, assembly, handling, and mounting steps, due to their natural weakness. The authors consider that with a 0.635 mm pitch, there is a risk from 60 mm × 60 mm (which corresponds approximately to 370 I/Os).

BGA interconnection is not yet considered, due to the flatness requirements and to the coefficient of thermal expansion mismatches between BGA packages and PCBs. The rigid soldering assembly of BGA packages larger than 25 mm × 25 mm has a poor reliability. Moreover, after soldering on the PCB, the visual inspection of such assemblies is still a concern.

For these reasons, Astrium has developed Land Grid Array MCM packages for dematable interconnection, presenting a grid pitch of 1.9 mm × 5 mm and 1.9 mm × 1.5 mm. Due to that configuration, one can have a larger number of I/Os (up to 1000). The first MCM package developed with a Land Grid Array is dedicated to the DSP21020 processor. This hermetic package uses AlN material and a 100 µm HTCC technology. It uses also a dual configuration: peripheral leads and LGA which allows both to test the function through LGA without concerns about lead damages and conventional leads soldering onto the PCB. Its QFP configuration admits 340 leads at a 0.635 mm pitch (see Figure 4). The LGA configuration permits its interconnection to the PCB through the IUP interposer (described further). Currently, the LGA version, without leads, is developed and used in several applications.

In order to overcome the increase of MCM complexity, the concept of dual sided cavities has been developed. The solution consists to spread the I/Os on extended areas (wings) of the MCM...
package. Therefore, the ratio between the I/Os number and the package surface is optimized. This hermetic package uses also AlN material and a 100 µm HTCC technology. It admits 480 grid array pads on each side (see Figure 5). The Land Grid Array permits the interconnection to a PCB through IHD interposers. This kind of package permits also a 3D assembly (PCB to package and package to package) using IHD interposers.

Figure 5. Dual cavity MCM package. Top and back sides (58 mm x 78 mm x 7 mm).

5. Ruggedized MCM-VFL

A technology extension takes into account a “pseudo-hermetic” encapsulation in order to protect all dice and others from the environment. This concept allows avoiding the use of a ceramic package. It implies a significant benefit in terms of the following factors:

- mass saving (50%),
- cost (RE, NRE),
- manufacturing time, and
- electric signals (low parasitic effects).

3D-Plus, a French 3D-assembly company performed the upgrading of the encapsulated substrate by additional mineral layers. They developed a patented ruggedizing process to protect encapsulated substrates from harsh environment and more especially against humidity. Figure 6 shows a single sided substrate, equivalent in dimension to the dual sided package.

Figure 6. Ruggedized MCM substrate (58 mm x 78 mm x 2 mm).

The proposed process is composed of three-layer coating (see Figure 7). It can be used to protect encapsulated MCMs, PEMs, as well as COB system, and 3D modules from harsh environment and water diffusion.

Figure 7. Ruggedization - Principle.

The first coating is similar to a conformal coating and has different functions:

- Mechanical protection of the devices and of the bonding,
- Conformal surface state for increasing the sticking of the hermetic coating, and
- Smooth out acute angles.

This organic coating must show good adhesion to ceramic substrate, gold wire, and dice. This implies a low Coefficient of Thermal Expansion (CTE) to minimize the shear forces between the coating and the substrate with temperature. Epoxy resins filled with silica have been selected.

The second coating consists in a Silicon dioxide material. Only inorganic and metallic coatings have a diffusion coefficient low enough to ensure a hermetic packaging. It has been decided to deposit a silicon dioxide film that offers several benefits: it is transparent, colorless, it does not affect the polymer recycling, and moreover it has been extensively studied for its gas barrier properties against water and oxygen. The silicon dioxide ($\text{SiO}_2$) is deposited in a Plasma Enhanced Chemical Deposition (PECVD) 600 mm diameter reactor, from a hexamethyl disiloxane (HMDSO) liquid source. This technique permits to deposit silicon dioxide at room temperature with a very low electrode po-
potential and without damage for the devices. PECVD deposits of SiO$_2$ are known for their good adhesion to polymer substrates and their elasticity, up to 10% stretch without loss of barrier properties.

The third coating is an organic material consisting in a mechanical protection. Some materials have been qualified. Parylene coating is the most useful, particularly for microelectronic hybrid applications.

Evaluation of the hermetic coating reliability has been performed using pressure cooker test and permeation measurement. Adhesion of the silicon oxide film onto the epoxy resin encapsulant permits to obtain a good barrier against water diffusion. During the deposition parameters set up, the silicon oxide coatings sticking on epoxy resin substrate, has been tested using different techniques: Pressure Cooker Test (PCT: 2 atms, 121°C and 99% RH), scratch test performed after PCT, thermal cycles (-55 to +125°C). Only free acid anhydride epoxy resin shows no blistering defects after PCT. This epoxy resin was selected as conformal coating for the 3D Plus process.

A study was carried out in order to find out what process parameters lead to the optimal sticking of the silicon oxide coating on this epoxy resin. It was observed that the sticking could be drastically improved by submitting the epoxy surface to very low energetic plasma before depositing the silicon oxide. This treatment is close to a polymeric surface reticulation. An optimization of the treatment parameters was performed and a silicon oxide deposition process showing satisfactory silicon oxide coating adhesion to epoxy resin is obtained. No cracks, blisters, or pilling off after 500 thermal cycles, PCT treatment and scratch test are now observed on optimized silicon oxide.

Both elasticity and gas barrier properties of the silicon oxide films were optimized too. The elasticity of the silicon oxide film was tested by PCT, whereas gas barrier property was tested by permeation measurement through a 500µm thickness epoxy substrate. It has been measured that the typical 27105 cm$^3$/m$^2$/day/atm oxygen permeation value obtained through the epoxy sheet, is drastically reduced to 0.11 cm$^3$/m$^2$/day/atm due to the presence of the 0.5 µm silica film. This represents a more than 3×10$^6$ gain! Compared to traditional ceramic packages, the ruggedizing process can be defined as an equivalent hermetic technique.

Consequently, this encapsulation and ruggedization study shows that reliability without hermeticity is achievable using commercially available high purity epoxy resin materials. The MCM-VFL technology together with advanced plastic encapsulated microelectronics provides a reliable packaging approach to meet the demand for “better, faster, cheaper, and smaller” spaceborne electronics.

### 6. Interposers

The PCB interconnection to large ceramic package or to another PCB has been developed at ASTRIUM. It is based on a Grid Array area both on ceramic package and on PCB, and defined by the following specifications:

- Compliant with Space environment,
- Compliant in term of bending and warping (100 µm/inch)
- with large ceramic package,
- Easy mate/demate,
- Possible stacking (package on package),
- No insertion force, and
- Possible full custom connector.

Two connectors have been defined and named:

- IUP interposer (see Figure 8) characterized by a low profile (2 mm thick).
- IHD interposer (see Figure 9) characterized by a low pitch (1.9 mm × 1.5 mm).

![Figure 8. IUP interposer (not at scale).](image)

![Figure 9. IHD interposer (not at scale).](image)

Table 1 presents the main connectors properties. The IUP interposer is compliant with single sided MCM LGA packages. The interconnection between the MCM package and the PCB is located on the backside (as shown on Figure 4).

<table>
<thead>
<tr>
<th>Pitch/Depart</th>
<th>Contact Resistance</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>IUP 5.0×1.9mm</td>
<td>&lt; 20 mΩ</td>
<td>2 mm</td>
</tr>
<tr>
<td>IHD 1.9×1.5mm</td>
<td>&lt; 20 mΩ</td>
<td>7 mm</td>
</tr>
</tbody>
</table>

Another interesting feature is the testability of MCM package. Several packages, developed by Astrium, integrate a mixed connection: leads and Grid Array area. The IUP connector is used to connect the package directly on a PCB, like Plug&Play, in the frame of Burn-In and three temperatures test. The
DSP21020 processor, as shown on Figure 4, is tested with this new connector (334 I/Os). This mixed interconnection option has been made on customer requirements. Therefore, the leads are protected by a carrier (see Figure 4) and are not damaged during handling and test.

The IHD interposer is compliant with single sided and dual sided MCM package. It is dedicated to the interconnection of complex MCMs with more than 900 I/Os (as shown on Figure 5). This interposer is developed in collaboration with a connector manufacturer and intended to become a connector off-the-shelf. Its applications are numerous, from interconnection of dual cavity MCM package to a PCB, up to the stacking of several MCM packages. The interconnection between PCBs and more especially between daughter and mother PCBs represents another application of IHD interposers.

A campaign of evaluation has been led in order to assess these connectors for Space applications. Two configurations: MCM package / IUP / PCB and PCB / IUP / PCB have been tested. The IUP and IHD interposers were evaluated with the following tests;

• 1000 hours @ 125°C under 0.5 Amp. / contact,
• 500 thermal cycles (−55°C / +125°C),
• 96 hours 85°C / 85% HR,
• Sinus vibrations from 10 Hz to 4000 Hz, and
• 100 Mate / Demate cycles.

The interposers passed all these tests with success, their contact resistance is lower than 20 mΩ. The IUP and IHD interconnections are compared in terms of MCM package size and number of I/Os to leads. As shown on Figure 10, the IUP interposer is more efficient in term of I/Os than a 0.635 mm pitch, 60 mm × 60 mm and than a 0.5 mm pitch, 80 mm × 80 mm leaded packages. As shown, the IHD interposer is also efficient from a 60 mm × 60 mm package.

The first packaging application at Astrium is dedicated to payload processors. A prototype has been developed in order to perform the evaluation of the main features of this architecture in term of thermal capability and densities. The results have been compared to those obtained on conventional digital equipment. This prototype is voluntarily limited to three daughter board locations. It is described on Figure 1 and shown on the graph illustrated in Figure 11.

![Figure 11. Prototype equipment.](image)

About thermal dissipation, due to the large ASICs mounted inside each MCM, up to 80 W can be generated on each daughter board. Due to the original brackets used to maintain pressure between MCMs interposers and PCB, a less than 2°C/W thermal resistance has been observed between the ASIC dice and the equipment base plate. Several solutions are being studied to reduce this value.

About integration density, there are several means to define it and to compare the performances obtained both with a conventional structure and the 3D modular packaging. In the following comparison, it has been considered that the main parameter to evaluate integration density is the total surface of silicon of all active components assembled, both as packaged components and as bare dice. Consequently, all the active components are considered as bare dice and several packaging efficiency parameters have been evaluated. In each case, packaging efficiency is evaluated as the ratio between the total silicon surface of all components present inside the equipment and an other characteristic of the equipment, for instance weight, volume, PCB surface, among other characteristics. This result depends also on the modularity and the number of daughter boards in the equipment. In the following, the authors provide two results, corresponding to 1 and 12 daughter boards.

Packaging efficiency in volume is given as total silicon surface (in cm²) / global equipment volume (in liters), for 1 daughter board and for 12. Packaging efficiency in mass (weight is an important parameter for Space) is given as total silicon surface (in cm²) / global equipment weight (in kg), for 1 daughter board and for 12. One can see that in each case, a benefit of more than 5 is obtained when using the new architecture. Packaging efficiency on PCB is given as total silicon surface / total PCB surface and is expressed in (%), for each daughter board. This comparison leads to a factor of 10 between the two solutions. As high density PCBs must be used to interconnect very dense MCMs, their routing capability can also be evaluated in terms of packaging efficiency. Routing efficiency is given as total tracks length / PCB surface, for each daughter board (in cm/ cm²). At last,
connectivity efficiency is given as the maximum number of possible contact points between each daughter board and the mother board.

8. Conclusions

It has been seen that the new 3D Modular Packaging structure shown in this paper presents a lot of improvements in comparison with a more conventional equipment structure in use in Space applications. A lighter ratio weight/volume (1 kg/liter for this structure compared to 2.4 for a conventional one) is an important improvement, especially in Space applications for which the launching cost of weight is very expensive. Moreover, it has been seen that two times more active silicon can be integrated in the same volume. Thermal performance is good and a power dissipation of 1 W/ASIC die or 80 W/daughter board leads to an increase of temperature limited to 15°C. But, some enhancements at the material level could reduce this value at a lower level.

Beyond all these benefits, it remains that the two more important improvements due to this novel architecture and particularly to the dematable connections induced by the use of both IUP and IHD interposers are the following,

• the test, the screening and the reworkability of MCMs, integrated inside large packages,
• the reliability towards temperature cycling of these same large packages.

One can now conclude that this novel 3D Modular packaging architecture represents an important improvement in regard of Space applications, particularly for the future high density digital telecommunication payload processors. Figure 12 shows the highly radiation tolerant MCM DSP 21020 developed by Astrium and qualified for Space applications. This DSP is already in use on Rosetta and available for Flight Models.

Figure 12. MCM DSP 21020.

References


About the authors

Dr. Michel R. Massénat is currently employed at Astrium, in charge of advanced micropackaging studies. Previously, he was an ASIC Design Engineer at Schlumberger, Commercial Engineer at Philips, and Quality Engineer in the Assembly technologies sector at Matra. He received a Ph.D. in Electronics from Bordeaux University. His recent research and development activities have been in the areas of Multichip Modules, Chip Size Packages and Inspection. He is author of numerous papers and studies for the European and French Space Agencies. He wrote a French book on Multichip Modules and is presently Expert to the European Community.

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