BGA Reliability of Multilayer Ceramic Integrated Circuit (MCIC) Devices

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Abstract

Multilayer ceramic integrated circuit (MCIC) devices using low temperature cofired ceramic (LTCC) technology have advantages in the wireless applications attributed to the unique RF materials’ properties and ease of multilayering leading to high Q RF devices. In this paper, the reliability of MCIC-BGA was evaluated under thermal cycling and mechanical test conditions. Two commercial metal pastes were used for each prototype: pure silver and mixed silver/palladium. Accelerated thermal life tests and several mechanical tests were conducted for two prototypes of MCIC devices with three BGA configurations of each. Three-dimensional nonlinear Finite Element analyses were conducted to simulate the thermomechanical and purely mechanical responses under the test conditions. The test data and Finite Element results were correlated, and failure sites were examined. The study shows the reliability of MCIC with silver paste outperforms that of MCIC with mixed silver/palladium paste. Enough silver print and eutectic tin-silver solder are recommended in assembly line to maintain acceptable reliability.

Key words:

Ball Grid Array (BGA), Reliability, Multilayer Ceramic Integrated Circuit (MCIC), Accelerated Thermal Life Test, and Finite Element Analysis.

1. Introduction

The multilayer ceramic fabrication process represents a robust fabrication technology for creating a variety of highly integrated circuit structures useful in the electronics industry. The basic multilayering process has been and is currently being used to manufacture multilayer devices such as ceramic passive devices, multilayer ceramic capacitor (MLC), substrates for electronic packaging applications, and hybrid circuit fabrication, packages for digital circuit multichip interconnect applications, sensors for gas detection in the automobile industry, and structures for fuel cell applications. This study is focused on the emerging application of low temperature cofired ceramic (LTCC) multilayer ceramic devices for the RF consumer portable wireless market. The unique RF properties such as high dielectric and metal Qs and low temperature coefficient of frequency (Tf) enable low cost and highly integrated devices demanding many levels (such as 10-30 layers) are featured. Within Solid State Research Center (previous Ceramic Technology Center) of Motorola, this version of the multilayer ceramic fabrication technology is being advanced to integrate components essential to creating and supporting RF circuit functions requiring the integration of capacitors, resistors, transmission lines, and inductor coils. The thrust is called Multilayer Ceramic Integrated Circuits (MCIC) to avoid confusion with other multilayer ceramic technologies such as MLCs products and multichip ceramic modules (MCM) interconnect packaging products.1

Ball Grid Array (BGA) interconnect has become an important technology for semiconductor products for both device I/Os as well as package I/Os due to the following advantages: good reliability, reduced demands on coplanarity, self-centering; good PCB assembly yields, high interconnect density (higher I/Os for
a given circuit footprint), and fast design-to-production cycle time\(^2\). Many of these same features are attractive to the MCIC RF application as well.

Silver and silver/palladium metallization with tin/lead and tin/silver based solder are probably the most commonly used interconnect material system in MCIC (LTCC) or in thick film assembly. The effects of tin and silver diffusion and intermetallic formation on the solder joint strength and fatigue fracture between the interface of Ag/Pd metallization and the Sn/Pb or Sn/Pb/Ag solder have been observed\(^3\). However, direct reliability discussions between silver and silver/palladium metallization with various solder systems are missing. In this paper, the authors evaluate these two metallizations with eutectic tin/silver solders. The studies include accelerated thermal life and for two MCIC prototype designs, each with two metallizations, three mechanical tests with different metallizations and solder systems. Even though the reliability issues regarding silver migration of silver-based materials under humidity condition are also important, these are not covered in this study. Material characterization using a Scanning Electron Microscope (SEM) was also conducted. Several nonlinear Finite Element analyses were also performed to support the study. Ultimately, life predictions can be flexible to RF designs and less time and cost consuming.

2. Experimental Procedures and Finite Element Modeling

2.1. Board Level Thermal Accelerated Life Tests

The tests were performed for Design 1 with Dupont 6139 AgPd and Design 2 with 6132 Ag metallization under \(-40^\circ\) to \(85^\circ\)C air-to-air thermal cycles with a 30min. hold time at each extreme. The transition was about 20 min. For each Design, there were three geometrical configurations. For Design 1, the configurations being studied include 10.4mmx 9.14mm MCIC with 5x5 BGA of 0.89mm (35mil), 0.51mm (20mil), and 0.38mm (15mil) solder heights. 96.5Sn3.5Ag solder was used to attach the non-collapsible solder balls. For Design 2, the configurations being tested included 10.16mmx8.89mm MCIC with 9x7 BGA of 0.38mm (15mil) heights of non-collapsible solder balls with 0.41mm, 0.46mm, and 0.51mm metal pad size. All of the solder joints were connected in one daisy-chain fashion. Failure was defined when, during thermal cycling, 10X of resistance changes. However, the data (resistance) were not monitored continuously. After failure was observed, the cross sections of failed joints were examined with a Scanning Electron Microscope (SEM).

2.2. Mechanical Tests

The integrity of MCIC-BGA interconnects with Ag and Ag/Pd metallizations were also evaluated by a three-point bending test to a PCB with a Design 1 piece, solder joint pull tests, and ball shear tests. The first tests were shown in Figure 1 and were to evaluate the strength of combining solder shearing and stretching. Solder paste of 96.5Sn3.5Ag is used. Direct solder-joint pull tests, as shown in Figure 2, were able to approximate the bond strength of pure ball stretching and were performed for Design 1 using three solder pastes with different extent of silver scavenging to tin-based solders: 96.5Sn3.5Ag, CASTIN (96.2Sn-2.5Ag-0.8Cu-0.5Sb), and 10Sn88Pb2Ag under different reflow conditions. The effect of reflow cycles on the solder joint integrity was also examined. 1X, 5X, and 9X of reflow processes were examined. The Sebastian ball shear tester was used to evaluate the bond shear strength. Two solder pastes, 96.5Sn3.5Ag, and 62Sn36Pb2Ag, were applied for Design 1 with Ag metallization.

2.3. Finite Element Modeling

The analyses were performed using a commercial ANSYS™ software package. The materials were all assumed linearly elastic, except for solder alloys. In this paper, the rate-dependent (creep) behavior of 10Sn90Pb and 96.5Sn3.5Ag solders were decoupled from the plastic (rate-independent) deformation. With the assumption of infinitesimal deformation, one may have,

\[
\sigma_{ij} = C_{ijkl} \varepsilon_{kl} = C_{ijkl}(\varepsilon_{kl} - \varepsilon_{,kl})
\]
where $C_{ijkl}$ is the stiffness matrix and can be obtained from elastic constants of the materials (given in Table 1). The inelastic strain rate, $\dot{e}_k$, is the sum of the plastic strain rate, $\dot{e}_p$, and the creep strain rate, $\dot{e}_c$. The mechanical properties of silver/palladium are approximated from those of the silver.

Table 1. Material elastic constants.

<table>
<thead>
<tr>
<th>Material</th>
<th>Coeff. of Thermal Expansion (ppm/°C)</th>
<th>Young’s modulus (GPa)</th>
<th>Poisson ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dupont 951</td>
<td>5.8</td>
<td>152*</td>
<td>.17</td>
</tr>
<tr>
<td>silver</td>
<td>19.2</td>
<td>72</td>
<td>.34</td>
</tr>
<tr>
<td>63Sn/37Pb</td>
<td>22</td>
<td>28</td>
<td>.45</td>
</tr>
<tr>
<td>10Sn/90Pb</td>
<td>28</td>
<td>21.1</td>
<td>.4</td>
</tr>
<tr>
<td>copper</td>
<td>16.5</td>
<td>117</td>
<td>.34</td>
</tr>
<tr>
<td>PCB</td>
<td>25* (in plane) 63(out plane)</td>
<td>17.23</td>
<td>.3</td>
</tr>
<tr>
<td>*measured in CTRL</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The material non-linearity is defined by two ANSYS data Tables for each solder: one for bi-linear isotropic hardening (temperature dependent) plasticity and the other for creep, which is expressed by the power law, as follows,

$$\Delta \varepsilon_{cr} = B * \sigma^n \ e^{(-\Delta Q/RT)} \Delta t$$

The parameters for material non-linearity are listed in Table 2. Note that in general, high lead solder such as 10Sn90Pb, is softer, and has lower yield strength and flow stress than SnPb eutectic solder. In the Finite Element modeling, the authors have neglected the stress relaxation of the solder joint during the 30min dwell time. A rate-independent constitutive model of the solders was used in this work.

Table 2. Inelastic parameters.

<table>
<thead>
<tr>
<th>Plastic Parameter</th>
<th>63Sn37Pb</th>
<th>10Sn90Pb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yield strength (MPa)</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td>Tangent moduli (MPa)</td>
<td>117</td>
<td>117</td>
</tr>
<tr>
<td>Yield strength (MPa)</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Tangent moduli (MPa)</td>
<td>70</td>
<td>70</td>
</tr>
<tr>
<td>T=-40°C</td>
<td>35</td>
<td>35</td>
</tr>
<tr>
<td>T=-10°C</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>T=0°C</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>T=20°C</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>T=60°C</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>T=100°C</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>Creep Parameter</td>
<td>$B^*$</td>
<td>$n$</td>
</tr>
<tr>
<td>-------------------</td>
<td>----------</td>
<td>----------</td>
</tr>
<tr>
<td>$6.62 \times 10^{-3}$</td>
<td>5.25</td>
<td>5689</td>
</tr>
</tbody>
</table>

3. Results and Discussions

3.1. Finite Element Results

Figure 3 displays the fringe patterns by the Moiré Interferometry technique for the PCB in-plane ($U_x$) and out-of-plane ($U_y$) displacement fields for the Design 1. The sensitivity of the images is 417nm per fringe order. Since the fringe pattern gives the relative displacement, any point in the image can be used as the reference of the relative displacement calculation. Figure 4 shows the contour plots of the two-dimensional plane-strain modeling for the module subject to the same temperature excursions using the rate-dependent material models. (Note: The numbers of the contours in simulations are not the same as those of Moiré fringes.) The differences between the measured and the simulated results are 7.1%, and 9.6%, for the in-plane, and out-of-plane cases, respectively, as can be shown in the locations circled on the Figures. Simulations were also performed using the rate-independent material model. The discrepancies of the rate dependent and rate independent simulations are only 0.4%, and 1.6%, for $U_x$, and $U_y$, respectively.

Based on these results, one may use the rate-independent material laws for the rest of the simulations to save computer time. The results verify the material properties as well as the finite element models used in this study.
3.2. Results of Board Level Thermal Life Test

Figures 5 and 6 show the Weibull plots of solder joint failure versus the number of thermal cycles for Design 1 and 2 (−40°, to 85°C), respectively. The mean cycle to failure (MCTF) for Design 1 can be calculated and has the range from over 200 to just below 600. At the time, one may have only 38% of failure for the case of Design 2 over 1000 cycles. This is comparable with the LTCC Chip Scale Package (CSP) reliability study from Unno et al.11. With the results of the corresponding Finite Element analyses, the Coffin-Manson reliability curves for Designs 1 and 2, which relates component life and the fatigue parameter (the inelastic strain range), were plotted in Figure 7. It shows that the reliability curves of Designs 1 (with Ag/Pd as MCIC metallization) and Design 2 (with Ag as metallization) are significantly different. For the same level of inelastic strain range, the life from the curve of silver (Design 1) is much higher than that of silver/palladium (Design 2).
3.3. Mechanical Tests

The displacement-control three-point PCB bending tests were conducted to compare the strength of two MCIC metallizations, Ag and Ag/Pd, with eutectic SnAg solder paste. Results showed BGAs with MCIC Ag/Pd metallization can bear only one third of the load, when compared with Ag metallization. The failure distributions of the samples with Ag/Pd and Ag metallization were plotted in Figure 8. The strengths of the joints were around 37 MPa, to 48 MPa, for AgPd, and Ag, respectively. The latter falls into the published strength of 47 MPa to 53 MPa at higher strain rates (>0.004s⁻¹) for 93.5Sn3.5Ag solder from CINDAS material database. This implies the failure may be at the solder or at the interface of silver/solder or silver/MCIC. However, when Ag/Pd is used, the joint is highly possible to fail at the weaker interface of metallization/solder or metallization/MCIC.

Among the solder pastes in the shear tests, the joints with eutectic SnAg solder have better shear strength than the 62Sn36Pb2Ag solder (20 MPa versus 16 MPa), but worst than that of an Ag-enhanced solder paste which was developed in-house (28 MPa). This behavior be shown in Figure 11.
The results of the solder-joint pull tests on Ag/Pd metallization were shown in Figure 12. The reflow conditions 1, 2, and 3 stand for as-reflow for each solder paste, four times, and eight times of 221°C reflow, plus original reflow, respectively. Despite 10Sn88Pb2Ag has better silver scavenging resistance than Sn-Ag solders as reported by Bulwith, the solder joint integrity with eutectic SnAg, and the CASTIN solders are still better than that with 10Sn88Pb2Ag as long as enough metal thickness is maintained.

![Figure 12. Solder-joint pull tests with three solder pastes under different reflow conditions.](image)

### 4. Conclusions

The model and material properties used in the thermomechanical simulation of BGA on MCIC have been established and verified by the Moiré method. In the board-level thermal cycling tests, the mean cycle to failure for Designs 1 and 2 can be estimated by the Weibull model. The data together with the Finite Element results can be fitted in Coffin-Manson equations. This plot can be used to predict the likely MCTF of a new design using the modeling results. It showed there is a significant reliability improvement if Ag is replaced by AgPd, assuming both are subject to comparable thermomechanical responses.

SEM cross sectional images of the Design 1 show that complete reaction of the Ag/Pd metallization with the tin/silver solder after reflow, and a continuous layer of Ag metal and AgSn intermetallics for Ag version. From the SEM images, the researchers also observed that the MCIC metallization diffuses to the Tin-base solder and its thickness decreases. The strategy to improve the reliability of the BGA solder joints is to increase the bond strength of the joints by a thicker conductor print, selecting better metallization for MCIC and solder paste system with better Ag leaching resistance. In the process of improving the interconnect metallurgy of the BGA solder joints, 96.5Sn3.5Ag was found to have better strength and re-workability. The MCIC metal pads to receive the BGA preferably use Ag instead of mixed Ag/Pd.

### Acknowledgment

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### References

11. H. Unno, H. Ishikawa, and Y. Kudo, “Highly reliable Ceramic Carrier For CSP Using Low Temperature Cofired Ce-
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About the authors

Chia-Yu Fu received his Ph.D. Degree from the Georgia Institute of Technology in Mechanical Engineering. He joined the Ceramic Technology Research Lab, (CTRL), a part of the Solid State Research Center (SSRC) of Motorola Labs in 1998. He has been involved in mechanical characterization, computational techniques, and Finite Element modeling of microelectronic packaging systems. Chia-Yu is currently working on multilayer ceramic process modeling, packaging systems for Ceramic Microchannel Electrical Mechanical Systems (C-MEMS), and Multilayer Ceramic Integrated Circuits (MCIC). He has filed two patents. He is a member of IEEE CPMT and IMAPS.

Rong-Fong Huang received a B.S. Degree in Earth Science from National Cheng-Kung University, Taiwan, a M.S. Degree and a Ph.D. Degree in Ceramic Engineering from University of Missouri-Rolla. Dr. Huang joined Motorola’s research organization in 1984, and had conducted formulation, processing, and device R&D related to sensors, piezoelectric, oxide superconductors, and low loss dielectrics. Since 1991, he championed the development of multilayer ceramic integrated circuit for RF wireless application and its production transfer. Dr. Huang holds 16 US patents and has published numerous papers in the field. He is a contributing Editor for the Journal of the Ceramic Society and a Motorola Distinguish Innovator award recipient. Dr. Huang was the manager of the Electronic Material System Technology when the work related to this paper was done. Currently, he is an executive of Aimta, Inc., a technology development company located in Fremont, California.