Flip Chip Joining on FR-4 Substrate Using ACFs

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Abstract

Anisotropic conductive adhesive films (ACF) were used to attach daisy-chained test chips on FR-4 substrates. The feasibility of ACF joining was studied since it is a potential method for fine-pitch bare-die attachment on low-cost organic substrates. Four types of test chips were used, each having a pitch of different size. One of the chips had an area array structure, one had a staggered structure, while the others had a peripheral structure. The reliability of the flip chip joints was evaluated by subjecting the test chips to a temperature cycling test and to a preceding reflow aging test. The joints were studied by electrical measurements and scanning electron microscope. The alignment of the chips was confirmed with an x-ray microscope.

Low resistance values were obtained in the flip chip joining process. However, it is evident that coplanarity of the substrate and the chip is important for the bonding quality. During the reflow aging test and the reliability tests some of the tested samples seemed to fail due to stresses that had induced during the bonding process. The reason for the failures was a too high bonding pressure. By decreasing the bonding pressure, reliability of these test chip types was improved.

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Key words

Anisotropic Conductive Adhesive Film, Flip Chip, FR-4, Reliability, ACF

1. Introduction

Anisotropic conductive adhesive films (ACF) have been successfully used to join driver circuits on liquid crystal displays [1]. Using ACFs, reliable high-density interconnections have been made also on flexible substrates [2]. Use of rigid organic substrates in adhesive flip chip attachment is an interesting alternative for making high-density interconnections. However, cost-effective manufacturing will require reduced bonding cycle times and/or use of multyhead joining equipment.

Long-term reliability of adhesive joints on organic substrates is a key factor to be ensured. Coplanarity of substrate and chip is important for the achieved bonding quality. Warpage and bump height variation in the organic substrates may cause problems that do not occur when even glass substrates are used. The challenge, however, is to achieve a uniformly low contact resistance that is stable over time at environmental stresses.

In this study, daisy-chained test chips were attached on FR-4 substrates using anisotropic conductive adhesive films. Large test chips were chosen to maximize stresses induced by CTE (Coefficient of Thermal Expansion) mismatches between chip and substrate during thermal cycling. Hard nickel bumps were used to stress the problems due to non-homogeneous substrate. The effect of chip structure on the reliability of the assemblies was studied using four test chip types with different layouts.

2. Performance of joints

It has been shown that best reliability of adhesive flip chip joints is obtained when conductive particles are deformed uniformly [3]. Uniform deformation is affected by uniformity in bump and pad height, homogeneity in particle size, and coplanarity between chip and substrate.

In addition to uniform deformation, the degree of deformation of the conductive particles has a great influence on reliability of adhesive flip chip joints. An adequate pressure is needed to form good joints, but an excessive pressure may cause crushed particles and decreased reliability by producing elastic stresses [4]. Furthermore, reliability of adhesive joints is affected by the degree of curing of the adhesive matrix. Full cure is needed to obtain stable electrical properties and good peel strength of the joints [5, 6].

Bump material, conductive particle material, and compatibility of the bump and particle materials play an important role in assembly yield and reliability. Bumps can be of different metallurgies, like Au, Ni/Au, and Cu. Conductive particles, on the other hand, can be rigid metal particles, like Ni particles, or compliant metal-coated polymer spheres. Results show that using an ACA containing hard Ni-particles a flip chip with Cu bumps has higher assembly yield than a flip chip with Ni/Au bumps [7]. This may be due to the microhardness, which is larger for the Ni/Au bump and prevents the particles from penetrating into the bumps and pads. Good results with Ni/Au bumps have been obtained when an adhesive filled with compliant Au-coated polymer spheres has been used [7, 8].

Carefulness and tight contamination control in the bumping process are required to obtain good bump quality and high yield in the
assembly process. For example, cracks in a passivation layer under Ni-bumps have been reported [7].

Coplanarity and homogeneity are the most critical parameters when replacing the flat glass substrate with less controllable printed circuit board [9]. Plastic deformation of the bumps and the substrate can compensate for some of the coplanarity issues since bonding takes place under pressure and high temperature [9]. On the other hand, high bonding temperature used in conductive adhesive assembly can cause problems that do not occur in soldering assembly. High bonding pressure and high bonding temperature which exceeds the glass transition temperature of epoxy may cause FR-4 substrate behave like a cushion during the bonding. It has been shown that joints close to glass fibers have better reliability compared with joints far from fibers since glass fibers stiffen the structure of the substrate [10].

It has been shown that the pad finishing material affects the assembly yield of adhesively bonded flip chips on FR-4 substrates. Organic-coated copper (OCC) has reported to give better results than Ni/Au-coated copper when an adhesive containing hard Ni-particles is used [7]. This may be due to the less curved surface of the OCC coating [7]. In addition, Ni-particles sink into the OCC pads, which may help to compensate for small height variations. On the contrary, hard Ni/Au-coating on top of the pads behaves like an anvil and prevents the particles from sinking into the pads. In the case of compliant metal-coated polymer spheres, which do not sink into the pads and thus do not penetrate through the finishing material, Ni/Au-coated copper pads may work better, since the resistivity of the Au-finish is much lower than the resistivity of the OCC.

3. Experimental Procedure

Test samples were made by attaching test chips on FR-4 substrates with ACFs. The conductive adhesives used were commercial epoxy-based adhesives. Table 1 presents the composition of the adhesives. The test substrates were of glass epoxy composite having copper wiring with electroless Ni and flash Au finishing. Four different kinds of test chips were used, all 10mm x 10mm in size. All the test chips were silicon chips containing electroless Ni/Au bumps. Pitch, number of bumps, and layout structure of the chips varied. Chips 1 and 2 had peripheral structures with pitches of 200 mm and 300 mm, respectively. Chip 3 had an area array structure with a pitch of 400 mm (200 mm in the outermost row), while chip 4 had a staggered structure (two rows) with a pitch of 250 mm. Each test board contained 20 test chips in total.

The chip assembly was made with a Toray FC-1000 flip chip bonder. First, the adhesive film was cut to the appropriate length and was placed onto the cleaned substrate. Pre-bonding was performed with the flip chip bonder by applying moderate heat and light

<table>
<thead>
<tr>
<th>Particles</th>
<th>Adhesive A</th>
<th>Adhesive B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Particle φ</td>
<td>Au coated polymer ball</td>
<td>Au coated polymer ball with insulation</td>
</tr>
<tr>
<td>Bonding temperat.</td>
<td>190 °C</td>
<td>160°C / 180 °C</td>
</tr>
<tr>
<td>Bonding time</td>
<td>25 s</td>
<td>15 s / 15 s</td>
</tr>
<tr>
<td>Bonding pressure</td>
<td>B1: 92 MPa</td>
<td>B4: 138 MPa</td>
</tr>
<tr>
<td></td>
<td>B2: 120 MPa</td>
<td>B5: 158 MPa</td>
</tr>
</tbody>
</table>

Table 1. Composition of the conductive adhesives and the used bonding parameters for both adhesive types.
pressure recommended by the manufacturer of the adhesive. The cover sheet was removed and the final bonding was made with the flip chip bonder using the bonding parameters presented in Table 1. Two different bonding pressures were used for both adhesive types.

After assembly, daisy chain resistances of the assemblies were measured using a HP3458A multimeter. Reliability of the joints was studied by subjecting the assemblies to temperature cycling. Temperature cycling tests were performed in two conditions. The first test was carried out between temperatures -30°C and +85°C for 500 cycles. The second test was more severe reaching from -40°C to +125°C for 500 cycles. Duration of exposure at the temperature limits was 14 minutes and the transition time was 3 minutes. After the tests and a period of stabilization at room temperature, the resistance values were measured again to evaluate the effect of environmental stresses on the resistance of the joints.

Resistance to reflow treatments is needed since new electronics applications may include components that are soldered on the substrates after the adhesive flip chip bonding process. To evaluate the effect of the reflow treatment on the reliability of the assemblies, half of the test boards were subjected to a conventional Sn/Pb reflow process. After the reflow aging, the test boards were subjected to the temperature cycling test, and the test results were compared with those of the other test boards.

### 3. Results and discussion

The measured resistance values are shown in Table 2. The resistance of one joint was approximated by dividing the measured daisy chain resistance value by the number of the bumps in the chain. This value, however, consists of resistances of a Al track on the chip and a Cu track on the substrate in addition to the contact resistance of the joint. The resistance values shown in the table are average resistance values for each chip type. As can be seen in Table 2, better results were achieved with adhesive A.

With chip 2 there were some problems during the bonding process. Several open circuits were found. The formation of the open circuits did not depend on the bonding pressure used or on the adhesive used. All these assemblies were constructed under the same conditions. For the successful assemblies the measured resistance values were comparable with the resistances of the other chip types. However, the average contact resistance values for the test chips 2 were noticeably greater due to a large value range.

### Table 2. Average resistance value per joint after the bonding process.

<table>
<thead>
<tr>
<th>Adhesive</th>
<th>Chip 1 (mΩ)</th>
<th>Chip 2 (mΩ)</th>
<th>Chip 3 (mΩ)</th>
<th>Chip 4 (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B1 70</td>
<td>147</td>
<td>90</td>
<td>73</td>
</tr>
<tr>
<td></td>
<td>B2 83</td>
<td>194</td>
<td>98</td>
<td>75</td>
</tr>
<tr>
<td>B</td>
<td>B4 171</td>
<td>272</td>
<td>119</td>
<td>116</td>
</tr>
<tr>
<td></td>
<td>B5 134</td>
<td>283</td>
<td>119</td>
<td>119</td>
</tr>
</tbody>
</table>

The alignment of the failed test chips type 2 was inspected with an x-ray microscope, but it was noticed that all the chips were aligned accurately. As a conclusion, the formation of bad joints was also considered to be the result of the substrate warpage or the bump height variation. The board planarity in terms of height variations in attachment areas was measured with a UBM-Microfocus Compact
laserprofilometer. As a result, no significant differences were observed between different sites on the test boards, but occasionally the variation in height seemed to be greater than the diameter of the conductive particles. Furthermore, the failed chips were evaluated with a scanning electron microscope (SEM). Figure 1 presents a micrograph of two failed joints in a test chip 2. As can be seen, overetched copper pads caused at least one failure. Overetched pads lead to insufficient contact formation between conductive particles and bump and pad surfaces. Figure 2 shows that, in this case, there was no contact formed between pads, bumps, and particles at all. An example of a good joint can be seen in Figure 3.

Figure 2. An overetched pad and an open joint.

Figure 3. A good flip chip joint.

The change in the average joint resistance values under the environmental exposure conditions can be seen in Figures 4 to 7. All the chips having resistance values per one joint over 1 ohm were considered as failed. As can be seen in Figures 5 and 7, test chips having staggered and area array structure, i.e test chips 3 and 4, failed in the reflow test. However, test chips 1 and 2 with peripheral structure seemed to withstand the thermal shock. The resistance values of the specimens attached with adhesive B even decreased during the reflow aging process. The decrease in the joint resistance during heat treatment may be a sign of an undercured adhesive. As the curing of the adhesive proceeds, the adhesive shrinks and the conductive particles are deformed more, increasing the contact area and decreasing the contact resistance.

After the milder temperature cycling test, more failures were observed in the test boards that were subjected to the reflow process prior to the temperature cycling test. Totally 30 % of
**Figure 4. Reliability of the test board B1 (Adhesive A).**

**Figure 5. Reliability of the test board B2 (Adhesive A).**
Figure 6. Reliability of the test board B4 (Adhesive B).

Figure 7. Reliability of the test board B5 (Adhesive B).
the test chips in the test boards B2 and B5 failed during the test compared with the amount of 11% in the test boards B1 and B4. Since all the test chips 3 and 4 and 30% from the test chips 1 and 2 had failed so far, test boards B2 and B5 were left out of the severe temperature cycling test.

In addition to the reflow aging test, all the test chips 3 and 4 failed in the severe temperature cycling test. The reason for the failures was studied with a SEM and an x-ray microscope. It was noticed that the alignment of the chips 3 and 4 was not good enough. In fact, chip 4 was badly misaligned with overlap of pads and bumps less than 50%, as seen in Figure 8. As a result, alignment was corrected, and new assemblies with good alignment were bonded. Test chip 4 was used in the new test procedure. The test chips were joined using adhesive A and a bonding pressure of 92 MPa. In addition, a few samples were bonded using a lower bonding pressure of 77 MPa. After bonding, the test chips were subjected to a temperature cycling test from 40°C to +125°C. During the first 250 cycles, all the chips that were attached with the higher bonding pressure failed. The average joint resistance of the passed chips that were attached with the lower pressure was 179 mW, which is comparable to the joint resistance of the other test chips. Although it seemed that the original bonding pressure had been too high for the test chip 4, it was obviously not too high for the test chip 2, as can be seen in Figure 9, which shows a micrograph of sufficiently deformed particles. As a conclusion, it can be said that the bonding pressure recommended by the ACF supplier can only be treated as a reference, and a careful investigation with different bonding pressures must be performed for every application.

On the basis of the experiments with the test chip 4, it can be assumed that the reason for the failure of the test chip 3 was also too high bonding pressure. A careful investigation with a lower pressure value was performed for this chip type. Adhesive A was used again, and the bonding pressure was decreased to 70 MPa. After 500 cycles of temperature cycling from 40°C to +125°C, all the chips worked fine and the average contact resistance increased only slightly, as seen in Figure 10. The milder temperature cycling test was skipped since, in the previous test stage, the test chips 3 and 4 withstood it, while the severe temperature cycling test was critical.

Failure mechanisms were further studied with SEM. Figure 11 presents a micrograph of a joint in a test chip 3 bonded with the higher bonding pressure. The joint was opened during the severe temperature cycling test. Delamination of the adhesive layer from the chip interface is seen in the upper corners of the SEM micrograph. In addition, air bubbles were found in the adhesive matrix. The effect of air bubbles on reliability is not known, but for many open joints there were air bubbles around the bump or the pad. Air bubbles may decrease adhesion strength and underfill effect of the adhesive matrix. In addition, air bubbles absorb moisture, which may result in oxidation of conductive surfaces.
Figure 9. Sufficiently deformed particles in a test chip 2.

Figure 10. Results of resistance measurements with the test chip 3 and the lower bonding pressure.
4. Conclusions

Four daisy-chained test chips with different structures were attached on FR-4 substrates using anisotropic conductive adhesive films. Chips with area array and staggered bump layout failed in a reflow aging test and in a temperature cycling test from 40°C to +125°C. It seemed that the bonding pressure had been too high for these test chips, although the same pressure was not too high for the other test chips. Decrease in bonding pressure improved the reliability of these test chip types.

Thermal cycling resulted in some increase in contact resistance for every chip type. Delamination of the adhesive layer from the chip and substrate surface was due to shear stresses induced by CTE mismatch. In addition, elastic stresses caused by too high bonding pressure may have relaxed during thermal cycling, causing open joints. For many open joints there were air bubbles around the bump or the pad. The effect of air bubbles on reliability is not well known, but they seem to decrease the long-term reliability of adhesive flip chip joints.

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References


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