Transient 3D Heat Flow Analysis for High Power Insulated Gate Bipolar Transistors Using the Transmission Line Matrix

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Abstract

This paper presents a 3D transmission line matrix (TLM) implementation for the solution of transient heat flow in power devices. The miniaturization of electronic networks creates problems of heat dissipation. Good thermal management is therefore essential. Simulating power electronic systems presents peculiar challenges due to the need of detailed modeling of both circuitry and control algorithms. The Transmission Line Matrix method (TLM) is a powerful tool for analyzing thermal effect in electronic circuits and high power devices.

In this paper, thermal analysis for a 1200 A, 3.3 kV IGBT (Insulated Gate Bipolar Transistor) module was investigated and analyzed using the Three-Dimensional Transmission Line Matrix (3D-TLM) method. The results show a three-dimensional visualization of self-heating phenomena in the device, including the effect of the use of Metal Matrix Composite (MMC) materials as a base plate over conventional materials for electronic packaging thermal control and the use of the ceramics as substrates. This paper reviews the present status of the use of various thermal heat spreaders such as AlSiC MMC, Cu-Mo and Graphite-Cu MMC and comparing those to copper based heat spreaders. Also covered is the use of AlN, Diamond and BeO as substrates and their effect in dissipating the heat flux in heat sources localized in IGBT module designs. The effects of the geometry of the module and specific material thicknesses are taken into account because they play an important role in dissipating the generated heat and outweigh the thermal properties of the module.

The TLM method is found to be a versatile tool that is ideally suited to the modeling of many power electronic devices, and proved very useful in the study of transient thermal effects in a variety of device structures.
Keywords


1. Introduction

The solution of the heat diffusion equation using transmission line matrix (TLM) techniques is well established [1]. A specific application of TLM has been the solution of steady state and transient thermal responses of integrated circuit (IC) devices [2,3]. This problem is of substantial interest due to the need to know maximum operating temperatures for reliability reasons and to develop temperature-consistent models of the device.

Compactness and power handling capability of power devices in modern power electronics is currently being improved by hybrid power integration and related packaging techniques. Usually this leads to the use of single large area components or to parallel connection of several basic chips in order to build large power modules (e.g. high power Insulated Gate Bipolar Transistor) intended for railway traction applications [4].

Traditionally, the thermal management of these high power devices has been divided into two distinct levels. At the package or module level, handled by the manufacturer, the die is typically soldered to a ceramic substrate of high thermal conductivity, such as AlN, BeO, or Al₂O₃, which in turn is bonded to a flat metallic base plate that acts as both a rigid foundation for the electronics as well as an efficient heat spreader. At the system level, which is often left to the responsibility of the end user, a heat sink is needed to effectively dissipate the power from the package. This is typically accomplished by mechanically fastening the base plate to an aluminum or copper heat sink, consisting of either air-cooled plate fins, or to a flat water cooled cold plate with embedded circulation tubing [5]. Thermally induced stresses arising from difference in the coefficient of thermal expansion (CTE) of the various materials of this assembly can result in minor bowing at the module to heat sink interface, causing significant deterioration in the interface thermal performance.

Thus, an important trend for comprehensive device behavior simulation is to look for the 3D heat diffusion effects and their impact on the distribution of the load current over the cells. The most significant problem with this power electronic module concept is the issue of adequate thermal management and consequent electrical performance. With high power running through dense circuitry comes the undesirable side effect of an intense, concentrated heat source. This heat brings out two significant requirements that the materials within the module must meet in order for satisfactory operation to be obtained.

The first requirement is that the materials must have a high thermal conductivity in order to adequately dissipate the produced heat to the heat sink and the second requirement is that the material within the multilayer module must have matched low coefficients of thermal expansion (CTE) in order for the module to remain structurally intact. It is believed that a Metal Matrix Composite (MMC) heat spreader as base plate, with high thermal conductivity and low CTE has the potential to solve many of these thermal management issues [6].

In this paper, we analyzed the thermal effects in IGBT modules, focusing on the 3-D distribution of the temperature. Hence the thermal models were run through various simulations at various power levels under various conditions in order to obtain comparison graphs.
The series of simulations were performed in attempt to determinate the effects of heat spreaders such as AlSiC, Cu-Mo, Graphite-Cu and Cu at various thicknesses upon the maximum temperature of the module and under various load powers. The IGBT module exhibits different thermal behavior depending on the substrate material used. Materials such as Aluminum Nitride (AlN), Diamond and BeO have particularly good thermal conductivity. These ceramics provide electrical insulation to the underlying base plate, which is usually pressure mounted onto a heat sink by peripheral bolts [7]. The purpose the ceramic substrates is to decrease the self-heating in heat sources localized in IGBT module design.

In this paper, we propose the use of the TLM model to investigate the thermal behavior of a 1200A, 3.3 kV IGBT power module. We demonstrate that method has a considerable potential in thermal simulation and design of power semiconductors devices.

2. TLM Modeling of Heat Flow

Heat flow in a solid can be described by the equation:

\[ \nabla (k(T) \nabla T(x,y,z,t)) + H(x,y,z,t) = \rho_c \frac{\partial}{\partial t} \frac{\partial T(x,y,z,t)}{\partial t} \] (1)

where:

- \( T \) is the temperature
- \( t \) is the time
- \( H \) is the heat generation rate per unit volume
- \( \rho \) is the density
- \( k \) is the thermal conductivity.

This differential equation is discretized when simulating the physical process by a conventional numerical method. The TLM method is intrinsically a discrete approach that directly models a physical process. It has been shown that an electrical pulse on a transmission-line matrix obeys Maxwell’s curl equation for propagation in lossy medium, which has the form of the Telegrapher’s Equation [8]:

\[ \nabla^2 \Phi = AR_d C_d \frac{\partial \Phi}{\partial t} + BL_d C_d \frac{\partial^2 \Phi}{\partial t^2} \] (2)

where:

- \( \Phi \) is the potential
- \( R_d, C_d \) and \( L_d \) are distributed resistance, capacitance and inductance
- \( A \) and \( B \) are constants

If the first time derivative term on the right-hand side of Equation (2) dominates the second term, the network models the diffusion equation.

Therefore, it should be possible to model the thermal wave heat flow in terms of a lumped RLC network where temperature is represented by voltage. In the equivalent TLM network, as shown in Figure 1, the resistors remain clustered around the nodes and represent the thermal resistance of the material. The capacitor/inductor combinations are replaced by loss-free transmission lines of impedance \( Z \), which connect each node to its neighbors and carry voltage pulses between the nodes in finite time \( \Delta t \). According to the fundamental transmission line theory [9], the impedance is related to \( C \) and \( L \) through:

\[ Z = \frac{L}{\sqrt{C}} = \frac{a \Delta t}{C} = \frac{L}{a \Delta t} \] (3)

Since the capacitor model the heat capacity of the material, the TLM parameters \( R \) and \( Z \) can be evaluated from:

\[ 2R = \frac{1}{K_f \Delta x} \quad \text{and} \quad Z = \frac{a \Delta t}{\rho_c c_p \Delta x^3} \] (4)

where \( \Delta x \) is the length of the cubic elemental volume representing a node. The parameter \( a \) represents as well the number of link lines in each elemental volume.
A TLM solution is obtained by repeatedly considering delta voltage (temperature) pulses to be incident simultaneously on all parts of all nodes. These incident pulses are scattered instantaneously into reflected pulses which, during the time step $\Delta t$, travel along linked transmission lines to become incident upon neighboring nodes. The TLM routine operates on the traveling, scattering and connecting of these pulses in the network. The transmission lines in the model act as delay lines, with the node impulse population being the discrete solution at each time step [10].

From TLM modeling [2] the temperature at each node is given by:

$$
_k V(N) = \left[ \frac{2(kV_i + V_2)}{R_x + Z} + \frac{2(kV_3' + V_4)}{R_y + Z} + \frac{2(kV_5' + V_6)}{R_z + Z} \right] \frac{1}{Y}
$$

(5)

Where $Y = \frac{2}{R_x + Z} + \frac{2}{R_y + Z} + \frac{2}{R_z + Z}$ and

$kV_n'$ are incident pulses, at the $K^{th}$ iteration.

Reflected pulses are calculated according to:

$$
_k V_{1,2} = \frac{1}{R_x + Z} [Z_k V + (R_x - Z)V_{1,2}']
$$

(6)

$$
_k V_{3,4}' = \frac{1}{R_y + Z} [Z_k V + (R_y - Z)V_{3,4}']
$$

(7)
\[ V_{5,6}^{i} = \frac{1}{R_z + Z} \left[ Z V + (R_z - Z)V_{5,6}^{i} \right] \] (8)

These pulses travel to adjacent nodes to become, at the k+1 iteration, incident pulses given by:

\[ V_{j}^{i}(x,y,z) = \Gamma_{j} V_{j}^{i}(x,y,z) + \left(1 - \Gamma_{j}\right)V_{j}^{i}(u,v,w) \] (9)

Where (x, y, z) are node N co-ordinate and the reflection coefficient in direction (j) is given by:

\[ \Gamma_{j} = \frac{Z(u,v,w) - Z(x,y,z)}{Z(u,v,w) + Z(x,y,z)} \] (10)

The corresponding values of j', u, v, w for j = 1,2,..., of equations (9) and (10) are listed in Table 1 [2].

Implementation of a TLM routine consists solely of repeated application of Equations (5) to (10), accompanied by direction of pulses to appropriate neighboring nodes.

As argued by Kronberg and al. [11], boundary conditions express the interaction of the system hand with its surroundings. Boundaries are part of the transport model and thus should be consist with the description of the heat transport inside the medium. For a heat sinking boundary corresponding to an electrical short-circuit S/C and \( \Gamma_{j} = -1 \), any incident pulse on the boundary will be returned equal in magnitude but reversed phase. For a heat insulating boundary corresponding to an electrical open-circuit O/C and \( \Gamma_{j} = 1 \), any incident pulse on the boundary will be returned equal in magnitude and in phase.

3. The IGBT power module structure

The main criterion in the design of high power IGBT modules is to achieve a good thermal conductivity and a dielectric strength for the insulation between semiconductor devices (IGBTs and diodes) and a device header (base plate). Both parameters are primarily decided by the thermal and electrical characteristics of a substrate on which the semiconductor devices are mounted. The Figure 2(a) shows the schematic structure of the IGBT module (18.7cmx13.6cmx0.4cm), which, consists of six subassemblies using a Direct Copper Bonding (DCB) technique. This module has been developed in 1200A and 3.3kV ratings and was targeted specifically at the traction drives application [12]. One subassembly is constructed with semiconductor devices (4 IGBTs and 2 diodes) and a copper-mounted ceramic substrate. The thin film of copper is applied to the top and bottom surface of the ceramic substrate with good thermal conductivity. Six subassemblies are attached on the common base plate by soldering. This has mirror symmetry with respect to the center lines (both X and Y directions) of the substrate. Due to this symmetry, practical calculations were performed in the one subassembly with respect to the emitter size. For the numerical modeling, one sub-assembly (62mm x 68mm x 6.38mm) is considered and the restricted region of the IGBT module is modeled as shown in Figure 2(b).

The symmetry condition is used to generate an optimal set of geometric parameters that can meet the design objectives. The symmetry boundaries are represented by an electrical open circuit (O/C). A perfect heat-sink boundary is covered by the definition of the short-circuit (S/C) boundary of TLM [13].
Table 1. The Values of $j$, $j'$, $u$, $v$, and $w$ (Used for Equations (9) and (10))

<table>
<thead>
<tr>
<th>$j$</th>
<th>$j'$</th>
<th>$u$</th>
<th>$v$</th>
<th>$w$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>$x-1$</td>
<td>$y$</td>
<td>$z$</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>$x+1$</td>
<td>$y$</td>
<td>$z$</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>$x$</td>
<td>$y-1$</td>
<td>$z$</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>$x$</td>
<td>$y+1$</td>
<td>$z$</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>$x$</td>
<td>$y$</td>
<td>$z-1$</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>$x$</td>
<td>$y$</td>
<td>$z+1$</td>
</tr>
</tbody>
</table>

Figure 2 (a.) Schematic structure and (b) A restricted region of the IGBT module for the TLM modelling.

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Based on the thermal requirements, the ideal materials for the high power IGBT module must have high thermal conductivity. In addition, the combination of different materials must be compatible mechanically, i.e., excessive thermo-mechanical stress is not allowed to guarantee the long lifetime. The industry-wide standard heat spreader as base plate is Copper, due to its high thermal conductivity, Table 2 illustrates comparative material properties [14]. For the numerical analysis of the IGBT module, required material properties are listed in Table 3 [15].

Generally, with power dissipation occurring in two or more chips arranged on the common substrate, the lateral heat spreading effect can cause the thermal interference between the chips. Consequently it will accelerate the temperature rise. To predict the accurate temperature rise of Silicon chips, the chip thermal interference effect should be considered. Figure 3 portrays a simple substrate with 2 chips at a distance of 1mm, equal to the normal chip-to-chip distance. A heat source of 100W was applied only on the A-chip and B-chip without a heat source.

For all simulations, a program was written in Maple V language in order to evaluate the temperature at every node within the device as function of time and others parameters.

4. Results and Discussion

The transient thermal behavior of a power module can be illustrated by using three-dimensional views of distribution shows in simulation.

In the case of vertical power devices, where the thickness $L_z$ is small compared to other dimensions, it is commonly considered that heat is generated at the top surface of Silicon and flows uniformly along the $z$ axis (perpendicular to the Silicon surface). So, the top surface is considered to be a geometrical boundary of the device at $z=1$. The lower surface (at $z= L_z$) is considered to be the cooling boundary. Figure 4, shows the temperature profile along the vertical axis at the chip center with 100W thermal power. Shortly after the instant of 300$\mu$s, the Silicon device is initially heated and after instant ranging from 300 $\mu$s to 5 ms, the heat flux is flowing through the chip and is beginning to pass across the solder interface. The small amounts of temperature is noticed at the base solder region as shown in figure 4, so then the choice of a thin soldering layer under the Silicon devices and the base plate is advantageous.

In first the simulations were run with AlSiC base plate and AlN substrate. As expected, the thermal conductivity of the substrate is less than that of base plate, as is the case for the AlN substrate modules, the substrate acts as a thermal chokepoint, as shown in Figure 5.

Figure 5 displays the temperature distribution over the center of the device on X-Z plane containing the centers of the dissipation region. Regarding the IGBT module components, heat flows from the operating hot semiconductor devices to the base plate. The hottest spot temperature of 440$^\circ$K is observed in and around the centers of the IGBTs with 100W applied power dissipation. This peak temperature is found at the end of the channel region, where the current is high. However, the ceramic substrate and the base plate act as a heat spreader to dissipate the heat flux.

Figure 6 displays the surface temperature distribution in the middle of the base plate according to the source conditions because 100 W is applied in the IGBTs or in the diodes simultaneously. It is found that nearly all of the heat generated in the active region flows to
Table 2. Material property comparisons

<table>
<thead>
<tr>
<th>Materials</th>
<th>CTE (ppm/K)</th>
<th>Thermal Conductivity (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>3.0-4.1</td>
<td>100-170</td>
</tr>
<tr>
<td>AISiC</td>
<td>12.6</td>
<td>180-182</td>
</tr>
<tr>
<td>BeO</td>
<td>6.8</td>
<td>270</td>
</tr>
<tr>
<td>Copper</td>
<td>17</td>
<td>393</td>
</tr>
<tr>
<td>Cu-Mo</td>
<td>7.2</td>
<td>197</td>
</tr>
<tr>
<td>Graphite-Cu</td>
<td>2.0</td>
<td>356</td>
</tr>
<tr>
<td>Diamond</td>
<td>0.8-2.0</td>
<td>1000-2000</td>
</tr>
</tbody>
</table>

Table 3. Material properties of the IGBT modules, which are used in the thermal analysis

<table>
<thead>
<tr>
<th>Material</th>
<th>ρ</th>
<th>$K_t$</th>
<th>$C_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top plate</td>
<td>10220</td>
<td>138-159</td>
<td>255-293</td>
</tr>
<tr>
<td>Silicon</td>
<td>2320</td>
<td>148-156</td>
<td>700-753</td>
</tr>
<tr>
<td>Copper</td>
<td>8960</td>
<td>393-401</td>
<td>276-385</td>
</tr>
<tr>
<td>Substrate</td>
<td>3260</td>
<td>170-180</td>
<td>669-738</td>
</tr>
<tr>
<td>Solder</td>
<td>7400</td>
<td>40-50</td>
<td>160-220</td>
</tr>
<tr>
<td>Base Plate</td>
<td>2980</td>
<td>180-182</td>
<td>722-765</td>
</tr>
</tbody>
</table>

The lateral heat spreading effect causes the thermal interference between the IGBTs and diodes. Figure 7 shows the temperature profiles along three cross sections at three different points along X-directions. Even through there is not heat source in the B-Chip, the maximum rise of the temperature of approximately 20°C occurs through the P2 line. This is evidently caused by the heat source in the A-Chip. So this contributed temperature at the P2 line varies with applied power of the remote chip and the chip-to-chip distance.

After, two series of simulation were performed. The first series replaced the Copper heat spreader with various MMC materials of same dimensions, which were then compared as illustrated in Figure 8. The second series replaced AlN ceramic substrate of the DCB with various materials, which also compared as illustrated in Figure 9.
Figure 3. Simple structure for thermal interface

Figure 4. The thermal profile along the vertical axis at the chip centre. The small amounts of temperature are noticed at the base solder region.

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Figure 5. Temperature distribution over the central of the device on X-Z plane containing the centers of the dissipation region.

Figure 6. Simulated thermal distribution of the IGBT power module on X-Y plane.
Figure 7. The temperature profiles along three cross sections at three different points along X-directions

Figure 8. Heat spreader material comparisons
As can be seen from Figure 8, the Graphite-Copper material presents itself an extremely promising candidate as a heat spreader material. It has a thermal conductivity equaling that of Copper, while at the same time having a CTE of approximately 2.0 ppm/K which is much closer to Silicon that Copper’s CTE of 17 ppm/K to matching Silicon’s CTE of about 4.1 ppm/K. It can be seen that MMC material such AlSiC offers potential advantages in CTE matching and it is available on the commercial market, while Graphite-Cu is still in its experimental phases.

Figure 9 illustrates the enormous advantages of diamond material over today’s industry standard AlN or BeO ceramic substrates. Diamond offers an approximate 20% maximum power output increase over the AlN and BeO substrates and it had an excellent thermal dissipation capabilities.

Figure 10 illustrates a comparison of Copper and AlSiC MMC heat spreader materials with various thicknesses with AlN as substrate. The interesting conclusion that can be drawn, is that for all cases, the temperature performance levels off with a heat thickness of approximately 6 mm, regardless of load power or heat spreader materials and Figure 11 illustrates the effect of AlSiC heat spreader thickness upon the maximum module temperature under various load powers.

TLM has been successful in modeling heat diffusion problems and has proven to be efficient in terms of stability and complex geometry. The three-dimensional results show that method has a considerable potential in power devices thermal analysis and design.

5. Conclusion

Thermal management has served as a key enabling technology in the development of advanced microelectronic systems and has facilitated many of the advances in consumer products and high-performance electronic devices.

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Figure 10. Heat spreader thickness comparison

Figure 11. Maximum module temperature under various load powers
A three-dimensional numerical analysis has been presented to investigate the effect of self-heating in IGBT device.

The results show clearly that the IGBT modules are capable of self-generating considerable amount of heat that should be dissipated very quickly to increase device lifetime. Furthermore, the results shows that use MMC materials, ceramic substrate, the geometry of the module, and specific material thickness play an important role in dissipating the generated heat.

This work has also demonstrated that it is relatively simple to use the three-dimensional TLM method for thermal analysis of low dimensional semiconductor device structures. We believe that the unconditionally stable nature of the method and the ease with which complex geometry can be handled good with the TLM technique. So a comprehensive thermal analysis is possible for any power semiconductor device structure with complex geometry and fabricated with many different materials.

References


