The Symposium on Polymers for Microelectronics

Winterthur Museum & Gardens, Copeland Lecture Hall

14th Meeting Agenda

May 11-13, 2010

Tuesday **May 11, 2010**	**Session 1 - Wafer and Embedded IC Packaging**
8:30 - 8:35	**Welcome; Symposium Opening Remarks**
8:35 - 9:20	Chip Package Interaction; Jon Casey, IBM T.J. Watson Research Center, Yorktown Heights, NY
9:20 - 9:45	Impact of Chip-Packaging Interaction on Interfacial Cracking of Multilevel Cu/Low-k Interconnect Structures; Paul Ho; University of Texas, Austin, Texas
9:45 - 10:10	Chip-Package Interaction (CPI) and Chip Level Final Via Design; Timothy Daubenspeck; IBM, Burlington, Vermont
10:10 - 10:35	Polymer Requirements for Advanced Wafer Level Packaging; John Hunt; ASE, Phoenix, Arizona
10:35 - 11:00	**Break**
11:00 - 11:25	Polymer Nanocomposite Based Embedded Passives: Towards System in Package (SiP); Rabindra N. Das; Endicott Interconnect Technologies, Inc., Endicott, New York
11:25 - 11:50	Development of a Low Temperature Curing - Aqueous Base Developable Photoimageable Dielectric for WLP (Wafer Level Packaging) Applications; Michael Gallagher; Dow Electronic Materials, Marlborough, MA
11:50 - 12:15	Reduced Moisture Uptake and Moisture Expansion Polyimides; Garrett D Poe; NeXolve
12:15 - 1:30	**Lunch**
1:30 - 1:55	Ultra Low Temperature Curable Positive Tone Photodefineable Polybenzoxazole ; Tomonori Minegishi, Yamazaki R&D Center, HD Microsystems, Ltd and Hitachi Chemical Co.
1:55 - 2:20	Design of Novel Positive Tone Photosenstive Polyimide with High Sensitivity and Accurate Pattern Fidelity; Masao Tomikawa; Toray Industries
2:20 - 2:45	Cross-linking of Aqueous-Base Developable Photosensitive Polynorbornene; Mehrsa Raeis-Zadeh; Georgia Institute of Technology
2:45 - 3:10	**Break**
3:10 - 3:35	Ultra Low Temperature Curable Positive Tone Photodefineable Polybenzoxazole - II; Noritaka Matsuie, Yamazaki R&D Center, HD Microsystems, Ltd and Hitachi Chemical Co.
3:35 - 4:00	Underfill Material and Process Solution for Large Ultra Low K Flip Chip Encapsulaton; Marie- Claude.Paquet; IBM Bromont, Canada
4:00 - 4:25	Development of Thick Resist for Solder Bump; K.Mori, Yokkaichi Research Center, JSR Corporation
4:25 - 4:50	Reduced Warpage and Stress in Polymer Films for Microelectronics; Robert Hubbard; Lambda Technologies, Henkel Corporation, Department of Chemistry, University of Oregon

5:30 - 7:00	**Symposium Reception - Reflecting Pool**
Wednesday May 12, 2010	**Session 2 - 3D/TSV/Novel Apps**
8:10 - 8:55	Direction of Microelectronics in Chip Packaging Technology; Eric Beyne; ; IMEC, Leuven, Belgium
8:55 - 9:20	Integration of Thinned Silicon Chips into a Polymer-Copper- Redistribution- A-3-D Stacking Technology without TSVs; Tobias Baumgartner; Fraunhofer IZM
9:20 - 9:45	Evaluation of Photosenstive Spin-On Dielectrics for 3-D Wafer Level Packaging; F. Duval; ; IMEC, Leuven, Belgium
9:45 - 10:10	Coaxial Through Silicon Via for 3D Applications with Polyimide Dielectric; Richard Volant, IBM East Fishkill, New York
10:10 - 10:35	**Break**
10:35 - 11:00	Electrografted Polymer Layers for Insulation of Deep TSV Structures; V. Mevellec; Alchimer SA
11:00 - 11:25	Implementation of 3D Lithography for wafer Level Through Silicon Via (TSV) Applications; Alexander Feldman, Tessera, Israel
11:25 - 11:50	Temporary Wafer to Wafer bonding for 3D Integration using Polyimide Coatings; K.Zoschke, Fraunhofer Institute, Berlin, GE
11:50 - 12:15	Fabrication and Packaging of a Backside Contact, High Voltage Photovoltaic Device; Thomas Gorczyca; General Electric
12:15 - 1:30	**Lunch**
1:30 - 1:55	Wafer Level Via Filling and Interconnection Using Conductive Polymer by Screen Printing; Damien Saint –Patrice; CEA
1:55 - 2:20	Organic Optoelectronic Devices-Flexibility Versus Performance; Matt Aldissi; Universite de Limoges/CNRS, Fractal Systems
2:20 - 2:45	Novel Organosiloxane Polymers with Improved Device Properties; Edward W. Rutter, Jr.; Honeywell Electronic Materials
2:45 - 3:10	**Break**
	Session 3 - Electronic Materials and Methods
3:10 - 3:35	Thermal Contact Materials Requirements for Testing of Electronic Packages; ; Ashish Gupta; Intel Corporation
3:35 - 4:00	Using High Temperature Thermal Conductivity to Assess Reliability Performance of Epoxy Mold Compounds; Sheila Liza B. Dal; On Semiconductor Phillipines Inc
4:00 - 4:25	Printed Electronics-Fading into Reality; Donald Hayes; MicroFab Technologies, Inc. Plano, Texas
4:25 - 4:50	Polymer Process Optimization Made Easy; Clifford J. Hamel, SUSS MicroTec, Inc.
6:00 - 9:30	**Exhibitors/Cocktails/ Dinner**

Thursday **May 13, 2012**	**Session 3 - Electronic Materials and Methods**
8:00 - 8:45	Health Care Roadmap; Bill Burdick General Electric
8:45 - 9:10	Flexible Isotropically Conductive Adhesives with High Reliability and Mild Curing Condition; Dr. Cheng Yang; Department of Mechanical Engineering, The Hong Kong University of Science and Technology
9:10 - 9:35	Achieving Ceramic-like RF Capacitors Requirements with Organic based Materials; ; Jin-Hyun Hwang; Oak-Mitsui Technologies, LLC
9:35 - 10:00	Advanced Rework Solutions for Delectric Film Removal in Semiconductor Manufacturing Processes; Michael Phenis; Dynalloy
10:00 - 10:25	**Break**
10:25 - 10:50	Preventing Reliability and Yield Degradations Caused by Bubble Defects; J. Braggin; Entegris
10:50 - 11:15	High Speed Shear Testing of WLCSP Solder Alloys, and the Correlation to JEDEC Board Drop Testing; Andrew J. Schoenberg; Fairchild
11:15 - 11:40	Packaging Requirements for Flexible CIGS; Todd Tolliver; GE Research