Registration Form
Packaging Copper Workshop
December 15 - 17, 2003

$ave on the Technical Program Registration when you Register On-Line:
www.imaps.org/copper

Workshop Fees

	On/Before 10/31	After 10/31
❑ IMAPS	$515	$615
❑ Nonmember*	$615	$715
*Includes one-year individual membership in IMAPS		
❑ Speaker/Chair	$300	$400

Workshop Fees include an Abstract Book and a CD of Presentations. CD of Presentations will be mailed 10 business days after the event.

Additional Purchases

❑ Spouse/Guest Meals	$150	$150
❑ Add'l CD of Presentations (member)	$100	$100
❑ Add'l CD of Presentations (non-member)	$175	$175
❑ Shipping in the US	$7	$7
❑ Shipping Overseas	$25	$25

Housing ***(Hotel Cut-off is October 31, 2003)***

Housing Accommodations **must** be made directly to:
Red Lion Hanalei Hotel
2270 Hotel Circle North
San Diego, CA 92108
P: 800-882-0858 or 619-297-1101
www.hanaleihotel.com

Single/Double: $105
Please reference IMAPS when making reservations.

Payment (Register On-Line and $ave)

Registration Fee $____________
Additional Purchases $____________
Total Payment Due $____________

IMAPS Registration
611 2nd Street, NE
Washington, DC 20002-4909
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Merrifield, VA
Permit No. 1112

❑ Dr. ❑ Mr. ❑ Ms. IMAPS#__________

First Name________M.I.____Last Name________

Company/Affiliation________Job Position________

Address________________

City________State____Zip_____Country______

Phone__________Fax__________

E-mail________________

A $25 fee must be added to all Wire Transfers.

❑ Enclosed is a check payable in US funds to IMAPS
❑ Charge my fees to:
❑ Visa ❑ Mastercard ❑ Discover ❑ Amex ❑ Diners Club

Card #________________Expiration________
Signature________________

Card billing address, if different from above:

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Submit Registration and Payment

Mail this form with payment to: International Microelectronics And Packaging Society (IMAPS), 611 2nd Street, NE, Washington, DC 20002-4909. For credit card transactions, register on-line: www.imaps.org; or register by phone at 202-548-4001. Additional information? Email: IMAPS@imaps.org, or visit our web site: http://www.imaps.org. Cancellations will be refunded (less a $50 processing fee) only if written notice is postmarked on or before **Monday, December 1, 2003**. No refunds will be issued after that date.

IMAPS Advanced Technology Workshop on

Packaging Copper/Low-K Semiconductors

Red Lion Hanalei Hotel
San Diego, CA 92108
December 15 - 17, 2003

General Chair:
Dr. Andrew J. G. Strandjord, IC Interconnect
P: 719-533-1030 ext. 13
astrandjord@icinterconnect.com

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www.imaps.org/copper

Sponsored by:
The International Microelectronics And Packaging Society (**IMAPS**)

Early Registration and Hotel Deadline: October 31, 2003

IMAPS Advanced Technology Workshop on Packaging Copper/Low-K Semiconductors

Red Lion Hanalei Hotel

December 15 - 17, 2003

Monday, December 15

Registration: 11 am – 5 pm

Opening Remarks: 1:45 pm – 2 pm
General Chairs

Session I: Copper/Low-K

Session Chairs: Eric Beyne, IMEC; Scott Cummings, Dow Chemical

2 pm – 5 pm

Packaging Integration Issues with Low-K Dielectrics
Scott Cummings, Mike Mills, Joost Waeterloos, Dan Scheck, Dow Chemical

EMC Characterization for Improved T/C Reliability of Copper/Low K Chip Packaging
Min Yoo, Jiyoung Chung, Heeyoul Yoo, Kyeongsool Seong, Joonyeob Lee, Keunsoo Kim, Yoonjoo Khim, Seokho Na, Jinyoung Khim, Amkor Technology

Scaling of Thermal Conductivity and Mechanical Strength of Porous Low-K Dielectrics
Mihail P. Petkov, Jet Propulsion Laboratory; Tova Sardot, Manuel R. Zurbano, Nicholas Kioussis, California State University Northridge

Break: 3:30 pm – 4 pm

Rapid Reliability Assessment of ULSI Electronics with Copper-Low K Interconnects
Pat McCluskey, Shirish Gupta, University of Maryland

A Tale of Two Packages: Packaging Comparison for the Motorola MPC7410 PowerPC® Copper Processor
Linda Bal, Andrew Mawer, Motorola

Reception: 5 pm – 5:30 pm

Dinner: 5:30 pm – 7 pm

Tuesday, December 16

Registration: 8 am – 9:30 pm

Continental Breakfast: 8 am – 9 am

Session II: Materials

Session Chairs: Frank G. Shi, University of California – Irvine; Harry Fuerhaupter, Atotech Deutschland

9 am - Noon

Development of Low Stress Materials for Low-K Copper Integrated Circuit Packaging
Michael G. Todd, Larry Crane, George Carson, Jack Zhang, Vincent Villeda, Kathy Costello, Henkel Loctite Electronic Materials

Epoxy Molding Compound for Low-K Die
Shinichi Zenbutsu, Sumitomo Bakelite Co., Ltd.

Ultra Low-K Dielectric Insulators for On-Chip Interconnects: Materials Challenges and Potential Solutions
Willi Volksen, R. D. Miller, V. Lee, T. Magbitang, H. C. Kim, IBM Corporation

Break: 10:30 am – 11 am

Impact of Copper Low-K Materials on Advanced Interconnect Packaging
Surasit Chungpaiboonpatana, Frank G. Shi, University of California – Irvine

Electroless Ni/Au for Low-K Copper Devices - A Technology Roadmap
Thorsten Teutsch, Ronald G. Blankenhorn, Elke Zakel, PacTech USA - Packaging Technologies, Inc.

Lunch: Noon – 1 pm

Session III: Handling/Assembly

Session Chairs: Michael Töpper, Fraunhofer IZM; D. Tonnies, SUSS MicroTec – Germany

1:30 pm – 4:30 pm

A Scribe and Saw Technique for Dicing Wafers with Low-K Dielectric/Metal Stacks
Pradeep Subrahmanyan, Electro Scientific Industries Inc.

Copper Electroplating Process with Improved Stability, Conductivity and Total Cost of Ownership
Harry Fuerhaupter, Robert Preisser, Thomas Dretschkow, Atotech Deutschland

Technology Enhancements in Full-Field Lithography to Meet 300mm Wafer-Level Packaging Requirements for Cu/Low-K Wafers
Klaus Ruhmer, SUSS MicroTec, Inc.; Dietrich Tonnies, Joe Kramer, SUSS MicroTec – Germany

Break: 3 pm – 3:30 pm

Composite Cost of Ownership of a 300mm Electroplating Bumping Line from UBM thru Singulation
Paul Siblerud, Semitool & Secap; Deitrich Tonnies, SUSS MicroTec – Germany

Electro-Chemically Deposited Copper for Packaging Applications
Bioh Kim, Tom Ritzdorf, David Erickson, Charles Sharbono, Semitool, Inc.

Reception: 5 pm – 5:30 pm

Dinner: 5:30 pm – 7 pm

Session IV: Wirebonding

Session Chairs: George Harman, NIST; Bob Chylak, K&S

7 pm – 9:30 pm

Packaging of Cu/Low-K IC Devices: A Novel Direct Fine Pitch Gold Wirebond Ball Interconnects onto Copper/Low-k Terminal Pads
Surasit Chungpaiboonpatana, Frank G. Shi, University of California – Irvine

Emerging Heavy and Fine Copper Bonding Wire for Chip Packaging
Z. Guo, L. Monterulo, C. V. Pham, K. Huth, Semiconductor Packaging Materials, Inc.

Automatic Copper Wire Bump and Ball Bonding
Bryan V. Drew, Palomar Technologies

Simulation of Wirebond Stresses under Bondpads in Copper/Low-K Technology
Kevin J. Hess, Susan H. Downey, Tom Lee, Lei L. Mercado, James W. Miller, Motorola

Successful Demonstration of Wire Bonding and Flip Chip Assembly on Cu-CVD Low K Interconnect
Tony Pan, Applied Materials; Jamin Ling, ST Assembly Test Services; Tom Strothmann, Jon Brunner, Frank Keller, K&S; George Carson, Renzhe Zhao, Henkel Loctite Corporation

Wednesday, December 17

Registration: 8 am – Noon

Continental Breakfast: 8 am – 9 am

Session V: Flip Chip

Session Chairs: R. Wayne Johnson, Auburn University; John U. Knickerbocker, IBM

9 am – Noon

Impact of Flip Chip Packaging on Interfacial Delamination in Cu/Low K Structures
Guotao Wang, Steven Groothuis, Paul S. Ho, University of Texas at Austin

Impact of Intermetallic Formation and Electro-Migration on the Integrity of Bumped Cu/LowK Dies
Riet Labie, Eric Beyne, Dominiek Degryse, IMEC

Finite Element Modeling of Shear Test on Bumped Cu-lowK Wafers
Dominiek Degryse, Riet Labie, Bart Vandevelde, Eric Beyne, IMEC

Break: 10:30 am – 11 am

Flip Chip Underfill Technology Development for Next Generation Silicon Technologies
Kumar Nagarajan, Kishor Desai, LSI Logic Corporation; Michael Todd, George Carson, Henkel Loctite

Bumpless Flip Chip Package for Copper/Low-K Semiconductor Devices
Charles W. C. Lin, Sam C. L. Chiang, T. K. Andrew Yang, Bridge Semiconductor Corporation

Concluding Remarks