15th International Conference and Exhibition on

DEVICE PACKAGING

MARCH 4-7, 2019
We-Ko-Pa Resort | Fountain Hills, Arizona USA
www.imaps.org/devicepackaging

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MONDAY, MARCH 4:
10 Professional Development Courses (PDCs)
Welcome Reception: 5:30pm-7:30pm

TUESDAY, MARCH 5-THURSDAY, MARCH 7:
5 Keynotes - 3 Tuesday and 2 Thursday Morning
GBC Plenary Session & Keynote Wednesday
Panel Discussion (Tues.) & Poster Session (Wed.)
Exhibits: 10am-6:30pm (Tues.), 10am-4pm (Wed.)
Innovative IC, SiP, and MEMS packaging portfolio to serve dynamic mobility, IoT, high performance computing, and automotive markets.

PoP • Flip Chip • SiP • WLP • Fanout • FOCoS
2.5D • TSV • Flex • AoP • AiP • Shielding
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Package it.

@asegroup_global  aseglobal.com
Welcome to Device Packaging 2019!

FROM THE GENERAL CHAIR

Jon Aday
Illumina, Inc., Sr. Staff Engineer

Welcome to the 15th International Conference and Exhibition on Device Packaging (DPC 2019) -- the premier annual conference where the latest in microelectronics system integration and packaging technology is unveiled. This week’s conference, organized by the International Microelectronics Assembly and Packaging Society (IMAPS), provides the stage to showcase the best in packaging technology available today, as well as those technologies soon to be released to the market. It offers the benefit of technical exchange among key international players and the opportunity to discover emerging business trends from top marketing analysts.

The conference provides a focused forum on the latest technological developments in four topical workshop tracks related to microelectronic packaging: Interposers, 3D IC and Packaging; Fan-Out, Wafer Level Packaging and Flip Chip; Engineered Microsystems and Devices (including MEMS and Sensors); and Automotive Packaging (New Track in 2019).

The 2019 conference will feature five premier technical keynote speakers, a Global Business Council (GBC) keynote and plenary session on the Transforming Power Packaging, and twelve technical sessions featuring more than 70 technical presentations all covering the latest in packaging technology innovation. Attendees will also enjoy a poster session and happy hour, a selection of ten professional development courses, plus a sold-out vendor exhibition and technology showcase. Gather with your industry colleagues for networking receptions and gatherings throughout the week, including the welcome reception, the exhibit hall reception, the poster session and happy hour, and a charity golf outing.

We are very excited about the program we have put together this year. Several key topics in our industry are being addressed with our keynotes, such as the requirements for artificial intelligence, heterogeneous integration, System-in-Package, and advanced fan out technologies. Benedetto Vigna from STMicroelectronics opens the conference discussing the future of sensors and Dr. Veer Dhandapani from NXP also gives a good preview of the automotive packaging space for our newest track. Jan Vardaman from TechSearch leads a panel discussion on Tuesday night on “Heterogenous Integration: Why Now?” that gets kicked off with a keynote from Sriram Srinivasan of Intel on packaging’s role in enabling heterogeneous integration. We are also excited to have a great second day of keynotes as Dr. Dan Oh from Samsung will discuss 2.5D and 3D integration for high end computing and using a fan out package for the mobile application processor. Dr. Raj Pendse from Facebook will wrap up the keynotes with a discussion on the packaging needs for AR/VR hardware which includes all the packaging techniques to make things smaller, lighter and more power efficient.

We hope you find great value in DPC 2019 this week in Arizona. Be sure to take it all in - visit sessions, attend keynotes, speak with all of the exhibitors, and NETWORK as much as you can!

Please utilize the mobile APP from your phone or tablet or visit www.imaps.org/devicepackaging for more updates. Contact IMAPS staff if you need any assistance.
Curious about the next advances in semiconductor packaging? Yeah, so are we. It’s that very curiosity that drives us to our next great material solutions that can help enable the next-generation technologies everyone else is curious to see. Let us know what you’re curious about.

Come see us at Booth #38
## Program at a Glance

### Monday, March 4:

**Registration:** 7:00 am - 7:00 pm  
**Professional Development Courses (PDCs):** 10:00 am - 5:30 pm  
**WELCOME RECEPTION:** 5:30 pm - 7:30 pm

### MORNING  Professional Development Courses (PDCs) – 10:00am-12:00pm

<table>
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<th>PDC1:</th>
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| **PDC1:** Introduction to Fan-Out Packaging  
Course Leader: John Hunt, ASE US, Inc. |

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<th>PDC2:</th>
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| **PDC2:** Introduction to System in Package (SiP) - The Heterogeneous Integration Driver  
Course Leader: Mark Gerber, ASE US, Inc. |

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<th>PDC3:</th>
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| **PDC3:** Flip Chip Package Technology and Assembly Processes  
Course Leader: Tom Dory, Fujifilm Electronics Materials |

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<tr>
<th>PDC4:</th>
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| **PDC4:** Polymers Used in Wafer Level Packaging  
CANCELLED |

### LUNCH  
**Only provided for those attendees registered for BOTH Morning and Afternoon PDCs**

### EARLY AFTERNOON  Professional Development Courses (PDCs) – 1:00pm-3:00pm

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<th>PDC5:</th>
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| **PDC5:** Advances in Fan-Out Wafer Level Packaging (FOWLP)  
Course Leader: Beth Keser, Intel Corporation |

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<th>PDC6:</th>
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| **PDC6:** Fundamentals of 3D and 2.5D Packaging Integration  
Course Leader: Urmi Ray |

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<th>PDC7:</th>
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| **PDC7:** Introduction to Solder Flip Chip with an Emphasis on Cu Pillar  
Course Leader: Mark Gerber, ASE US, Inc. |

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<th>PDC8:</th>
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| **PDC8:** MEMS and nanoMEMS Packaging  
CANCELLED |

### COFFEE BREAK IN FOYER

### LATE AFTERNOON  Professional Development Courses (PDCs) – 3:30pm-5:30pm

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<tr>
<th>PDC9:</th>
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| **PDC9:** Fan-Out Wafer/Panel-Level Packaging and 3D IC Heterogeneous Integration  
Course Leader: John Lau, ASM Pacific Technology |

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<th>PDC10:</th>
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| **PDC10:** Advanced Microelectronics Packaging  
Course Leader: Phil Garrou, Microelectronic Consultants of NC |

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<th>PDC11:</th>
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| **PDC11:** Introduction to Failure Analysis in Semiconductor Package Assembly  
Course Leader: Tom Dory, Fujifilm Electronics Materials |

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<th>PDC12:</th>
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| **PDC12:** 5G/mmWave Package Development Requirements and Solutions  
Course Leader: Urmi Ray |

### Tuesday, March 5

- 7:00 am - 7:00 pm  
  Registration

- 8:00 am - 9:55 am  
  Opening & Keynote Presentations  
  (ROOM 107-108)

- 10:00 am - 6:30 pm  
  Exhibits Open  
  (Wasaja Ballroom)

- 12:30 pm - 2:00 pm  
  Lunch Break In Exhibit Hall

- 2:00 pm - 5:30 pm  
  Technical Sessions - TA1-TA3

- 5:30 pm - 6:30 pm  
  Reception In Exhibit Hall  
  (Wasaja Ballroom)

- 6:30 pm - 8:30 pm  
  Evening Keynote & Panel Session on: HETEROGENOUS INTEGRATION: WHY NOW?  
  (ROOM 107-108)

### Wednesday, March 6

- 7:00 am - 6:00 pm  
  Registration

- 8:00 am - 12:00 pm  
  GBC Keynote & Plenary Session on TRANSFORMING POWER PACKAGING  
  (ROOM 107-108)

- 10:00 am - 4:00 pm  
  Exhibits Open  
  (Wasaja Ballroom)

- 12:00 pm - 1:30 pm  
  Lunch Break In Exhibit Hall

- 1:30 pm - 5:30 pm  
  Technical Sessions - WP1-WP3

- 5:30 pm - 6:30 pm  
  Poster Session & “Happy Hour”  
  Outside on Patio/Grass

- 6:30 pm - 8:00 pm  
  2019 3D InCites Awards Ceremony and 10th Anniversary Barbeque  
  Hosted by IMAPS

### Thursday, March 7

- 7:00 am - 11:30 am  
  Registration

- 8:00 am - 9:30 am  
  Keynote Presentations  
  (ROOM 107-108)

- 9:45 am - 11:45 am  
  Technical Sessions - THA1-THA3

- 11:45 am  
  Conference Ends

- 1:30 pm - 7:00 pm  
  IMAPS David Virissimo Memorial Spring Charity Golf Outing  
  Separate Registration - See Website or contact IMAPS Staff if you are interested to tee it up for a good cause!  
  WeKoPa Golf Club  
  1:30 pm Shotgun Start  
  “Scramble”
### THANK YOU TO THE DEVICE PACKAGING SPONSORS...

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Sigma
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Eliminate human error

Sigma HF
Higher force, higher speed, larger area
For forces up to 1000 kgf

Sigma XL
Large area bond tester
Working area of 500x500x200mm
Device Packaging Exhibition and Technology Showcase

Exhibiting Companies

The exhibit hall is now **SOLD OUT, marking this the 14th consecutive year of a sellout, and with more than 12 companies on a waitlist!** The following booths will be on display during Device Packaging 2019. Please visit the companies’ websites listed below for more information. The floor plan of the exhibit hall is included on the following page as well. If you have questions about exhibiting with IMAPS, or about getting signed up for the Device Packaging Conference Exhibitions, contact Brian Schieman at bschieman@imaps.org

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Shaping the Future

Applied Materials is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible™ the technology shaping the future.

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www.evatecnet.com
AdTech Ceramics is a fully integrated US based manufacturer of high temperature co-fire ceramic (HTCC) electronic packages and precision injection molded ceramic components. Standard ceramic materials offered include multilayer aluminum oxide and aluminum nitride. AlN is often preferred due to its excellent thermal conductivity and desirable coefficient of thermal expansion. AdTech also produces chemically or CNC milled metal components including package lids, leads and seal rings. Our injection molded products can be provided as fired, with metallization and plating or as full ceramic-to-metal assemblies. In our continuous drive for innovation and advanced technology for our growing customer base, we have recently added copper thick film metallization on alumina or aluminum nitride and ENEPIG plating capabilities. Located in Chattanooga, TN and with over 45 years of experience producing multilayer ceramic packages, we are ideally positioned to take on your most challenging package designs. Originally established as American Lava in 1903, AdTech has been owned by 3M, GE and Coorstek prior to its becoming Advanced Technical Ceramics Company in 2004. AS9100D/ISO9001:2015 certified and NADCAP accredited.

Advance Reproductions is a world-class provider of photomasking and photoplotting services, and unique photolithography solutions. Backed by a smart and creative technical team and driven by a commitment from the very first call to solving customers’ problems, we’ve built a reputation for delivering the most innovative photomasking solutions with high precision and speed. Most of all, our customers have the peace of mind that comes from knowing Advance is not just a provider of photomasking, photoplotting, and photolithography, but a company they can trust to successfully bring innovative product concepts to life for process engineers, photomask procurers, and university research centers worldwide.

Akrometrix is the worldwide leader of PCB and component thermal warpage metrology systems and test services utilizing Digital Fringe Projection (DFP), Shadow Moiré, and Digital Image Correlation (DIC) technologies utilized by various types of customers within the electronics industry. Our systems measure "at-room-temperature" warpage, thermal warpage [-50°C to 350°C], and thermal strain of substrates, materials, and electronic components/assemblies at critical reflow temperatures. Akrometrix systems provide graphical, statistical, and tabular results in order to help our customers comply to various industry standards.

AGC is a leader of glass, fluorinated polymers and synthetic quartz for the global automotive and electronics device industries. AGC provides specialized formulations of alkali-free aluminoborosilicate glass suitable for LED, MEMS, and interposer electronics substrates. Our high volume capability for glass and value-added services such as drilling vias, AR coatings, and via fill technologies makes AGC a valuable partner for your next generation mobile or Life Science product. AGC’s fluorinated polymer is ideally suited for dielectric coatings, or creating micro or nano-sized vias for Lab on a Chip applications in the Life Science technologies sector. AGC’s fluorinated polymer is highly transparent to 250 nanometers. It has the ability to change from a hydrophilic to a hydrophobic surface. AGC’s fluorinated material is the ideal candidate for passive and active coatings. AGC’s premier synthetic quartz with unparalleled formulation controls result in the lowest insertion loss and nearly zero auto fluorescence of any material. This provides our customers the highest electrical performance loss for high frequency circuits. In addition, AGC’s synthetic quartz’ low auto fluorescence makes it an excellent substrate for photonic applications in Lab on a Chip reactors.

AI Technology (AIT) developed flexible epoxies for microelectronic packaging in 1985. Today, AIT’s product line includes patented component, substrate and large die bonding adhesives and underfills, stack-chip packaging with dicing die-attach film (DDAF), flip-chip bonding and underfilling, single and multiple-chip module die bonding (230°C and above), and component and substrate bonding adhesives for military and commercial applications. AIT’s thermal interface materials, including phase-change pads, greases, gels and adhesives, ensure ultimate performance in semiconductors, modules, computers and communication electronics applications.
Alongside a broad portfolio of established technologies, OSAT industry leader ASE is also delivering innovative advanced packaging and System-in-Package solutions to meet growth momentum across a broad range of end markets. For more about our advances in SiP, Fanout, WLP, MEMS, Flip Chip, and, 2.5D, 3D & TSV technologies, all ultimately geared towards applications to improve lifestyle and efficiency, please visit: www.aseglobal.com.

ASMPT is the World Leader in Advanced Packaging Equipment Solutions, SMT Equipment, and Lead frame Materials. With a vision of providing customer focused cost effective solutions, we offer IC Assembly, Opto-electronic, Electronic Manufacturing, Physical Vapor Deposition / Chemical Vapor Deposition Equipment and Lead frame technology that is in the forefront of the Semiconductor Industry. ASM Pacific Technology is the only IC Assembly Equipment provider recognized as one of 2018 Thomson Reuters Top 100 Global Technology Leaders.

Axus Technology provides CMP, wafer cleaning and precision wafer grind process consulting services to emerging technology industries including MEMS, Automotive, Defense and Aerospace, Lifesciences and IoT as well as traditional semiconductor processing. The highly experienced Process Development team facilitates advances in wafer technology and efficient wafer production. We implement turnkey solutions for process development, foundry processing and equipment tooling including tool installation and training, field service and consumable selection.

Booth: 3
BSET EQ
Antioch, CA USA
www.bseteq.com

BSET EQ designs and manufactures gas plasma systems used for plasma etching, plasma cleaning, plasma surface treatment and plasma IC decapsulation for failure analysis and IC counterfeit detection. These dry processes are environmentally friendly and our systems are used worldwide in an increasing number of industries. BSET EQ is also the exclusive North American distributor for ATV Technologie GmbH IR vacuum solder reflow ovens and thermal processing systems. These systems range from small tabletop systems to high volume automated vacuum reflow systems. The product range also includes sintering presses, high vacuum Getter activation systems, atomic layer deposition systems, and diamond scribers. BSET EQ has both your plasma and thermal solutions, please visit us at booth 3 for more information.

Booth: 42
Cadence Design Systems
San Jose, CA USA
www.cadence.com

Cadence enables global electronic design innovation and plays an essential role in the creation of today’s integrated circuits, packages and PCBs. Cadence® IC packaging and cross-domain co-design automation provide efficient solutions in system-level co-design and advanced mixed-signal packaging, delivering the automation and accuracy to expedite the design process. Cadence also offers an integrated system design solution for TSMC’s advanced wafer-level Integrated Fan-Out (InFO) packaging technology. The solution includes implementation, signoff, and electro-thermal analysis tools that enable concurrent multi-chip optimization for designs incorporating InFO technology. With complex advanced packages, designers are faced with power integrity (PI) and signal integrity (SI) issues driven by increasing IC speeds and data transmission rates combined with decreases in power-supply voltages and denser, smaller geometries. Stacked die and packages, higher pin counts, and greater electrical performance constraints are making the physical design of semiconductor packages more complex. To address these issues, Cadence provides advanced PI and power-aware SI Signity™ tools that can be used throughout the design process.

Booth: 59
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CPS Technologies world leader and largest producer of AlSiC components, providing thermal management solutions, lighter weight, quick turnaround. CPS offers a full range of standard and custom Hybrid Packages including lighter weight AlSiC hermetic packages and complex Custom Machining’s for the Hi-Rel and Aerospace Industry! Participating Member of the JEDEC Committee, ITAR Registered, ISO 9001:2015 Certified, DFARS, RoHS and Reach Compliant. Please contact Cheryl Oliveira Tel: (508)222-0614x247, C Oliveira@alsic.com or Gregg Weatherman Tel: (714)612-7146 Email:gweatherman@alsic.com

Booth: 17
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Petaluma, CA USA
www.deweyl.com

DeWeyl provides the finest quality bonding wedges in the world. Located in the Petaluma, CA, DeWeyl’s primary business is manufacturing wire bond wedges and custom high precision tooling for the semiconductor, aerospace and medical industry. DeWeyl produces wedges made from ceramic, titanium and tungsten carbide for small and large round wire and ribbon applications.
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With the 2017 merger of Dow and DuPont, Dow Electronic Materials and DuPont Electronics & Communications have combined their portfolios and expertise to create the new DuPont Electronics & Imaging business, which is part of the new Specialty Products Division of DowDuPont. DuPont Electronics & Imaging is a global supplier of materials and technologies serving the semiconductor, advanced chip packaging, circuit board, electronic and industrial finishing, photovoltaic, display, and digital and flexographic printing industries. DuPont E&I’s portfolio includes metallization, dielectric, lithography and assembly materials designed to meet the most demanding needs for advanced semiconductor packaging applications, such as bumping, copper pillars and redistribution layer (RDL), passivation, underbump metallization (UBM), thermal interface and lid seal adhesion used for the latest fan-out wafer level packaging (FOOWLP), flip chip, system in package (SiP), and 2.5D/3D chip packages.

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DuPont Electronics & Imaging
Marlborough, MA USA
www.dupont.com/electronic-materials

Ev Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices, and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, Ev Group services and supports an elaborate network of global customers and partners all over the world. More information about EVG is available at www.EVGroup.com.

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Evatec NA Inc.
Cleanwater, FL USA
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Evatec delivers complete thin film production solutions for Advanced Packaging. From HEXAGON delivering FOWLP with the lowest Rc of < 1mOhm, the longest etch kit life and highest wafer throughput, to the PNL600 handling panel sizes >600mm it offers proven Fan-out solutions on both wafer and panel. For chip level EMI shielding our know how in soft magnetics, multi layer stack deposition with close management of temperature and high speed handling are combined on SOLARIS for a high throughput, compact platform with a low CoO. To find out more about Evatec thin film production solutions across all our markets of Advanced Packaging, Semiconductor, Optoelectronics and Photonics visit www.evatecnet.com. Alternatively call our local office in North America on +1 727 201 4313.

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F&K Delvotec is a leading supplier of wire bonders for all bonding technologies: gold-ball, thin wire wedge-wedge and heavy wire for gold, aluminum and copper wires. In addition, the revolutionary US laser bonder permits ribbon bonding of very large cross sections for high-current applications such as e-mobility battery pack manufacture. Highest bond quality is at the center of F&K Delvotec’s efforts. Unrivalled quality monitoring and controlling features, such as the patented Bond Process Control, permit real-time optimization of bond parameters while an individual bond is generated. Extensive SPC tools are available for thorough evaluation of bond processes and quick trouble-locating for process variations. F&K Delvotec stands out as a single-source supplier of equipment plus tailor-made automation solutions for an extremely wide range of industries such as microelectronics, automotive, sensors, semiconductors and many more.

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F & K DELVOTEC Inc.
Foothill Ranch, CA USA
www.fkdelvotec.com

FCI-HT supplies turnkey semiconductor assembly and test services to the consumer, automotive, industrial and medical industries. FCI-HT supports a wide range of customers, frequently partnering with them to engineer customized solutions including expedite bumping and backend services on Multi-Project Wafers. FCI-HT is a leader in wafer level packaging with patented technologies spanning from Cu Pillar Bumping, Spheron™ Wafer Level Chipscale Packaging, and ChipsetT™ Embedded Die Packaging. FCI-HT is a division of Huatian Technologies (HT). HT is among the top 6 OSATs in the world with over one billion dollars in annual revenue. It is listed on the Shenzhen Stock Exchange Market. Huatian has six ISO/TS16949 factories located in the US and China offering a complete range of semiconductor packaging and turnkey services.

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Gel-Pak manufactures a family of innovative Gel-coated boxes, trays, and films. Gel-Pak products are designed for applications where maximum protection is required for the shipping, handling and processing of valuable devices. Gel-Pak’s manufacturing expertise allows the company to quickly customize existing products and develop new solutions to meet ever changing industry requirements.
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- Largest OSAT in China
- Largest Industry Provider of Fan-Out Wafer Level Packaging
- Most Advanced SIP Capability in the Industry
- Pioneer in Advanced Flip Chip Technology
- IP Owner of Molded Interconnect System (MIS)

www.jcetglobal.com
If you’re looking for turnkey monolithic or hybrid assembly, fully compliant qualifications, complete burn-in services or any stage in between, you’ve found your answer. At Golden Altos, we’re committed to providing the semiconductor, military and aerospace communities with quality service building both single chip and multichip modules. Quality isn’t just a word at Golden Altos. We continually strive to deliver the finest products, services and documentation. We do this through our own internal quality system as well as regular certifications through outside and government agencies.

At IBM Assembly and Test facility in Bromont, we have asserted our proposition in several key areas providing solutions for high current and high thermal dissipation applications in computing electronics market and developing specialized areas with attractive know-how in RF, Antennas, SiP and advanced opto electronic packaging for communication and wireless markets. Beyond our technical orientation, our experienced engineering team takes pride in using its design, assembly and test expertise to provide tailor-made solutions for our client's needs and bring forth designs, prototypes and fast manufacturing ramp ups that are key to our client's success. Several fruitful collaborations have been enacted in the past months and we already have received feedback that it provides high value to the customers that have chosen us as their development and manufacturing OSAT solution. Clients also see value in our supply chain management proposition. Clearly beyond the customer-supplier relationship, we value true partnerships for mutual growth. We have an exciting product roadmap, some of the highlights include deploying high density interconnect laminates, pursuing integration and optimisation of SiP packages and also deploying technical milestones to prepare for dense optical integration which is highly anticipated by several key players of the communications market in the years ahead.

Booth: #29
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Booth: 65
KemLab Inc.
Woburn, MA USA
www.kemlab.com
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KemLab is a photosensitive manufacturer and photolithography research and innovation company located in Woburn, Massachusetts. We are focused on quality and cost-competitive high-tech photosensitive imaging materials used in the electronics industry. We offer Positive and Negative photoresists for advanced packaging, MEMS & Microfluidics, integrated circuits, metal lift-off, compound semiconductors, LED, image reversal, diffraction gratings, and sensor markets.

Booth: 50
JCET
Fremont, CA USA
www.jcetglobal.com

Jiangsu Changjiang Electronics Technology Co., Ltd. (JCET), the third largest OSAT in the world, provides innovative packaging and test solutions for semiconductor companies in well-established markets such as communications, consumer and computing as well as emerging markets in automotive electronics, the Internet of Things (IoT) and wearable devices. JCET offers customers a comprehensive and broad product portfolio that includes discrete, leaded, wirebond, flip chip, Micro-Electro-Mechanical Systems (MEMS) and sensors, Integrated Passive Devices (IPD), Molded Interconnect System (MIS), advanced wafer level packaging (WLP), Through Silicon Via (TSV) and System-in-Package (SiP) solutions. Headquartered in Jiangyin, China, JCET has an extensive global manufacturing base with operational centers in China, Singapore and South Korea and customer support offices throughout Asia, the United States and Europe. The JCET Group of companies also includes Jiangyin Changdian Advanced Packaging Co., Ltd. (JCAP) and Advanced Packaging (WLCSP) provider in China. JCAP’s broad set of capabilities include advanced wafer bump technology (copper pillar, gold and solder), wafer probe, WLCSP, Radio Frequency Identification (RFID), Encapsulated Chip Package (ECP) and Through Silicon Via (TSV) technology. JCET is a publically-traded company listed on the Shanghai Stock Exchange. For more information, visit www.jcetglobal.com
Kyocera Semiconductor Components Group offers a wide selection of semiconductor packaging technologies for medical equipment, database/servers, automotive, wireless/optical communication and consumer electronics industries. Technologies range from PCB and high density organic substrates to ceramic multilayer packages to epoxy molding compounds and die attach pastes. The combination of Kyocera's advanced material technologies, manufacturing processes and extensive design capabilities allow us to offer high-quality package and service solutions to meet the needs of our customers across a wide range of industries.

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Kyocera International, Inc.
San Diego, CA USA
https://americas.kyocera.com/kai-semiparts/

Booth: 49
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www.mentor.com/pcb/ic-packaging/

Mentor, A Siemens Business is the worldwide market leader in PCB systems design, advanced IC Packaging solutions and analysis technologies. Mentor will be showcasing its Xpedition High Density Advanced Packaging (HDAP) prototyping, design and verification solutions for heterogeneous multi-substrate designs such as FO-WLP, 2.5D and system-in-package. Visit booth #49 to learn more about Mentor's technologies and best practices for IC/Package/Board co-design.

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www.metalor.com

Metalor's Advanced Coatings Division is uniquely positioned as the only global source of precious metal commodities and plating solutions with manufacturing sites and refineries throughout US, Asia, and Europe. Our comprehensive plating process range includes precious metal solutions and ancillary products. Metalor offers gold, silver, platinum, palladium, rhodium, ruthenium materials designed for use in semiconductor, electronic, and decorative applications. We offer a complete service; the supply of precious metal replenishment salts and anodes, process chemistry, as well as refining services can be your one-stop provider for precious metal needs. Our Technical Service Team, located facilities worldwide, is on call and equipped to provide rapid response to specific customer queries as well as on-site installation support.

Booth: 43-44
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www.macdermidalectronics.com

Through the innovation of specialty chemicals and materials under our Alpha, Compugraphics, and MacDermid Enthone brands, MacDermid Alpha Electronics Solutions provides solutions that power electronics interconnection. We serve all global regions and every step of device manufacturing within each segment of the electronics supply chain. The experts in our Semiconductor Solutions, Circuitry Solutions, and Assembly Solutions divisions collaborate in design, implementation, and technical service to ensure success for our partner clients. Our solutions enable our customers' manufacture of extraordinary electronic devices at high productivity and reduced cycle time.

Booth: 7
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Metalor is a worldwide leader in adhesive technologies. For 30+ years, LINTEC has created equipment and materials to solve difficult semiconductor process issues. With a catalog of hundreds of tapes and equipment, and decades of application experience, LINTEC is positioned to help. Whether you are looking for tape, need equipment to mount, peel or UV cure - our staff stands ready to assist you to provide the Adwill Advantage.

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www.microchem.com

MicroChem develops and manufactures specialty chemicals including photoresists, dielectrics and ancillary materials for Packaging, MEMS, Microelectronics, Advanced Lithography, Specialty Displays, Packaging, Optoelectronics and other dynamic technology markets. MicroChem offers a broad range of resist and ancillary products to meet almost any applications need, including products such as PMGI and LOR bi-layer lift-off resists, SU-8 and KMPR® epoxy resists for various sacrificial and permanent imaging applications and PMMA resists for e-beam processing. In addition, we are the exclusive value added North American distributor for Dow Chemical's Semiconductor Technology (ST) and Advanced Packaging Technology (APT) resists, dielectrics and ancillary products.

Booth: 80
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MicroConnex = flexible electronics. MicroConnex offers fine-line flex circuits and laser microdrilling/machining. Capabilities include flexible printed circuits; high-density, fine-line, and fine-pitch (less than 2 mil trace/space); prototyping to production; laser-drilled blind, buried, and through-hole microvias; laser micromachining and drilling; and thin-film deposition.

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Micro Systems Technologies, Inc.
Lake Oswego, OR USA
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The MST group is specialized in developing and manufacturing miniaturized, integrated electronic module solutions. The capabilities include highly complex HDI/microvia PCBs, semiconductor packaging processes as well as advanced assembly in the field of SMT and chip & wire.
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Micross invites you to visit us at IMAPS Device Packaging, Booth 55. Micross will be showcasing advanced packaging solutions and their extensive range of interconnect & 3D integration technologies including 2.5/3D enabled applications; high density fan-out; image sensor technology; advanced assembly technology; bumping & copper pillar technology, equipment and materials. Micross provides full in-house state-of-the-art wafer bumping and WLCSP solutions. Whether you have a need to process a single wafer or are looking for a source to provide recurring production services, Micross has a wide array of WLP technologies. In business for 40+ years, Micross’ comprehensive array of hi-reliability capabilities serves the global aerospace, defense, space, medical, industrial and fabless semiconductor markets. Micross is the leading one-source provider of bare die & wafers, wafer bumping & advanced interconnect technologies, custom packaging & assembly, component modification services, electrical & environmental testing and Hi-Rel products to manufacturers and users of semiconductor devices. Learn more: Visit micross.com or email: onesource@micross.com

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www.mini-systemsinc.com

For over 44 years, MSI has been supplying superb quality and on-time deliveries. Absolute tolerances starting at 0.005% and TCR’s at 2ppm/C. Case sizes start at 0.01. Standard deliveries under 2 weeks. MSI is ISO 9001 certified and is on the QPL for MIL-PRF-55342 and MIL_PRF-32159.

Booth: 39
**NAMICS Technologies, Inc.**
San Jose, CA USA
www.namicsusa.com

NAMICS is a global technology leader for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells with over 70 years of experience and expertise. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China, NAMICS serves its worldwide customers with enabling products for leading edge applications. We build more than products: we build relationships setting the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application.

Booth: 36
**Neutronix Quintel (NXQ)**
Morgan Hill, CA USA
www.neutronixinc.com

Neutronix-Quintel (NXQ) is a leading provider of high performance mask alignment systems since 1978. NXQ is comprised of a team of seasoned industry veterans with vast experience in photolithography, providing their customers with the most robust solutions which have been derived from many years of customer driven innovations. NXQ has well over 1000 systems installed around the world used for various technologies such as MEMS, Compound Semi, Biomedical, Microfluidics, HB LED, WLP, 3DIC / TSV, 2.5D Interposer and HCPV. Prominent high volume manufacturing companies utilize NXQ’s equipment for end products such as transceiver chip sets for cell phones and other wireless devices, medical sensors, automobile sensors, LED Lighting, military and defence electronics, IR detectors, optical devices used for communications and discrete devices. The company’s products are also used extensively throughout the world at universities and research institutes and are recognized as one of the most versatile and flexible mask aligners in the marketplace. NXQ works closely with customers to innovate and develop new features that differentiate their products from the competition. The company continues to gain market share with customers that require equipment suppliers who can meet their stringent needs for cost, performance and reliability. With the recently release of the 300mm platform, NXQ is well positioned to maintain double digit growth.

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www.nordsonsonoscan.com

Nordson SONOSCAN is a leader and innovator in Acoustic Micro Imaging (AMI) technology. Nordson SONOSCAN manufactures acoustic microscope systems and provides laboratory services to nondestructively inspect and analyze products. Our C-SAM microscopes provide unmatched accuracy for the inspection of products for hidden internal defects in SMT devices, ceramic capacitors and resistors, hybrids, MEMs, etc.

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ORS provides a variety of Analytical Services to support Quality Control, Process Monitoring, Failure Investigation or Research and Development of your products. NOW OFFERING MECHANICAL AND ENVIRONMENTAL TESTING. As a leader in Residual Gas Analysis and Hermetic Testing, ORS can also supply test equipment for your in-house testing needs. ORS is a DLA suitable laboratory.

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Santa Clara, CA USA
www.ntktech.com

NTK Technologies is a leader in IC Ceramic Packaging. With global service centers, NTK offers a wide range of packaging materials and package design services for Medical, Automotive, SIP/MCM, MEMS, Opto, RF, CMOS Image Sensors, Hi-Rel, Satellite, FCBGA, FCCSP, FPGA, CPU and MPU applications. Monolithic package designs for Medical and Mobile applications. Optimum package designs for 10G, 40G, and 100/400G. Large and small scale Ceramic STFs are manufactured for high-speed/high density probe-cards for semiconductor wafer test. Large and small scale ceramic substrates can be configured with narrow pitches and a wide range of pin count capabilities. NTK supports fast paced product cycle times with our advanced design and production flows featuring high precision processes for fast turn-around with the highest quality.
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Booth: 25
PacTech USA Inc.

Booth: 9
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Brookfield, CT USA
www.photronics.com

Photronics is a world leader in sub-wavelength reticle solution technology as a result of its commitment to customer service, value and quality. Established in Connecticut in 1969, the Company became a publicly-held corporation in 1987. Today Photronics operates nine manufacturing facilities around the globe strategically located near the world's leading semiconductor and flat panel display manufacturers. We provide a complete array of photomask solutions for customers manufacturing semiconductors, flat panel displays, optoelectronics and data storage components. Our customer service and data prep staffs work around-the-clock to insure the best possible cycle time and quality.

Booth: 57
Plasma-Therm & Trymax
St. Petersburg, FL USA
www.plasmatherm.com

Plasma-Therm is a U.S. manufacturer of advanced plasma-processing equipment, providing etch, deposition, and plasma dicing technologies used in semiconductor packaging, solid-state lighting, power, data storage, renewable energy, MEMS, nanotechnology, photonics, and wireless communication markets. Plasma-Therm’s VERSALINE platform is the workhorse for a variety of applications in specialty semiconductor markets. The platform’s modular design allows flexible configuration of substrate handling and technologies that address the wide range of customer requirements. Plasma-Therm’s Singulator® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with “lab-to-fab” flexibility to meet the requirements of both R&D and volume production. Plasma-Therm’s products have been adopted globally and have earned their reputation for value, reliability, and world-class support.

Booth: 16
Palomar Technologies
Carlsbad, CA USA
www.palomartecnologies.com
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Palomar Technologies makes the connected world possible by delivering a Total Process Solution™ for advanced photonic and microelectronic device assembly processes utilized in today's smart, connected devices. With a focus on flexibility, speed and accuracy, Palomar's Total Process Solution includes Palomar die bonders, Palomar wire and wedge bonders, SST vacuum reflow systems, along with Innovation Centers for outsourced manufacturing and assembly, and Customer Support services, that together deliver improved production quality and yield, reduced assembly times, and rapid ROI. With its deep industry expertise, Palomar equips customers to become leaders in the development of complex, digital technologies that are the foundation of the connected world and the transmission of data generated by billions of connected devices. Palomar solutions are utilized by the world’s leading companies providing solutions for datacom, 5G, electric vehicle power modules, autonomous vehicles/LiDAR, enhanced mobile broadband, Internet of Things, SMART technology, and mission critical services. Headquartered in Carlsbad, California, Palomar offers global sales, service and application support from its offices in the USA, Germany, Singapore and China.

Booth: 31
Rudolph Technologies
Wilmington MA USA
www.rudolptech.com

Rudolph Technologies, Inc. is a leader in the design, development, manufacture and support of defect inspection, lithography, process control metrology, and process control software used by semiconductor and advanced packaging device manufacturers worldwide. Rudolph delivers comprehensive solutions throughout the fab with its families of proprietary products that provide critical yield-enhancing information, enabling microelectronic device manufacturers to drive down costs and time to market of their devices. Headquartered in Wilmington, Massachusetts, Rudolph supports its customers with a worldwide sales and service organization. Additional information can be found on the Company’s website at www.rudolptech.com.

Booth: 10
Practical Components
Los Alamitos, CA USA
www.practicalcomponents.com

Practical Components is an international supplier of dummy components (mechanical samples) which help engineers save money while improving their production processes, assists researchers explore emerging technologies and helps technicians test their production and recertify their skills. Practical dummy components not only have the same exact materials but are made on the same production lines as their live counterparts but without the costly die. Since 1996 Practical Components has been the exclusive distributor of dummy components from Amkor Technology. Practical Components® is also the sole agent for WALTS Co. LTD. extensive line of hi-technology products and provides advanced test element group wafers (TEG) die/test kits to the North American market. Our complete range includes over 40 different test wafers from Amkor and other manufacturers. Visitors can learn more about the company’s latest products including: Advanced Wafer Bumping Technology Chips and Test Vehicles, B-52 Rev B CRET (Cleanliness & Residue Evaluation Test) Kits, Amkor eWLP-Wafers .4 CuPd-DN 8” w/wafer-embedded copper pads, Amkor CSP-Wafers .4 DC-SAC405 8” wafers, 0.4 mm pitch, 3mm CVBG.

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Practical Components is an international supplier of dummy components (mechanical samples) which help engineers save money while improving their production processes, assists researchers explore emerging technologies and helps technicians test their production and recertify their skills. Practical dummy components not only have the same exact materials but are made on the same production lines as their live counterparts but without the costly die. Since 1996 Practical Components has been the exclusive distributor of dummy components from Amkor Technology. Practical Components® is also the sole agent for WALTS Co. LTD. extensive line of hi-technology products and provides advanced test element group wafers (TEG) die/test kits to the North American market. Our complete range includes over 40 different test wafers from Amkor and other manufacturers. Visitors can learn more about the company’s latest products including: Advanced Wafer Bumping Technology Chips and Test Vehicles, B-52 Rev B CRET (Cleanliness & Residue Evaluation Test) Kits, Amkor eWLP-Wafers .4 CuPd-DN 8” w/wafer-embedded copper pads, Amkor CSP-Wafers .4 DC-SAC405 8” wafers, 0.4 mm pitch, 3mm CVBG.
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SemiDice, Inc. is the preferred global wafer and bare die component supplier to the microelectronic industry. SemiDice is the only wafer processor with a High Reliability Division dedicated to providing bare die for military, aerospace, medical and robust industrial applications. Headquartered in the USA and with sales office in the UK and China ensures SemiDice is well-positioned to support customer requirements worldwide.

SETNA is a Manufacturing and Marketing, Sales and Service Organization centered on our experience and know-how in high-accuracy bonding and the equipment, materials, competencies surrounding it. SET Bonders have been the world-standard for applications in which micron precision post bond accuracy is required, for more than twenty years the FC150 Series has been the tool of choice. The Ontos7 is our atmospheric plasma system designed for and dedicated exclusively to the semiconductor manufacturing and packaging industry. Our patented (and patent pending) equipment and processes provide a unique advantage to our customers to enable low-cost, high yield, high-speed, chip-to-chip interconnect bonds at room temperature with minimal force.

StratEdge Company, founded in 1992, designs, manufactures, and provides assembly services for a complete line of high frequency, power, and high reliability semiconductor packages. They operate from DC to 63+ GHz for the high-speed digital, mixed signal, broadband wireless, satellite, point-to-point/multipoint, VSAT, and test and measurement industries. StratEdge offers post-fired ceramic, low-cost molded ceramic, and ceramic QFN packages and specializes in packages for extremely demanding gallium arsenide (GaAs) and gallium nitride (GaN) devices. All packages are lead-free and most meet RoHS and WEEE standards. StratEdge Assembly Services, in our new ISO 9001:2015 facility near San Diego, CA, has a Class 1000 cleanroom and Class 100 work area with workstations for performing sensitive operations. It is fully equipped with the most modern assembly equipment, enabling StratEdge services to include high-speed fine wire wedge and ribbon bonding for deep access. The new component placement die attach system is the fastest and most reliable multiple die-type bonder on the market. It enables StratEdge Assembly Services to offer high-accuracy and peak repeatability and performance. StratEdge has a variety of lids and options for their attachment and offers post assembly services.

Technic supplies some of the most advanced chemistry solutions for semiconductor fabrication and packaging in the industry. High-performance product development, with application specific characteristics and unparalleled analytical expertise, provides customers with the essential tools to meet the challenges of today’s semiconductor manufacturing. Technic’s semiconductor fabrication and packaging electroplating chemistries, marketed under the name Elevate®, are well respected for innovation and high quality. Elevate® processes offer high performing electroplating chemistries for copper, nickel, tin and precious metals. In addition, Technic supplies photoresist strippers for liquid and dryfilm resist as well as metal etchants and cleaners for a variety of substrates. Technic products provide a number of specific attributes that allow semiconductor manufacturers to remove many process limitations and take their technology to a new level. Our semiconductor fabrication and packaging chemistries are widely used in several advanced packaging platforms including FOWLP (Fan-Out Wafer Level Packaging), Fan-In WLP, Flip Chip and 2.5/3D.
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Higher Bandwidth, Higher Capacity, Thinner Profile, Lower Power, Lower Cost

Wafer to Wafer DBI® Hybrid Bonding

Die to Wafer DBI® Hybrid Bonding

Stacked 3D NAND with DBI

Stacked 3D DRAM with DBI

Benefits

- Periphery logic & memory array segregation - optimized manufacturing processes
- High Speed 3D NAND I/O performance, similar to DDR4 DRAM
- Faster product development and shortened manufacturing cycle time accelerates time to market

Benefits

- One stacking solution for all DRAM products
- 16 high stack can meet JEDEC HBM3 height specification
- Better performance, higher bandwidth
- Lower cost, lower profile, lower power & higher reliability

Contact Xperi for Hybrid Bonding Solutions
Invensas@xperi.com
For more than 25 years, Teikoku Taping System Inc. has been an innovative leader in custom equipment for the backend semiconductor industry.

Teikoku’s backend semiconductor products include Wafer Mounting Systems, UV Irradiation Systems, Tape Removal Systems, Backgrind Tape Laminators, and Dry Film Resist Laminators. TTS will continue to revolutionize the semiconductor industry and exceed industry expectations with new and innovative equipment designs.

Our core business is to support semiconductor manufacturers throughout the world with innovative solutions for plasma-based, photo resist removal and surface cleaning equipment, as well as isotropic etch systems that are used in the fabrication of integrated circuits and other semiconductor devices.

Trymax Semiconductor Equipment BV manufactures, sells and supports its own NEO equipment range. A wide range of different NEO platforms are available, from single chamber semi-automatic tools, through to multi-chamber high volume manufacturing platforms. Trymax offers a number of different NEO process chambers which are configurable across all NEO platforms. This enables Trymax to offer an extremely wide range of different etch, strip and surface modification process capability.

Unisem is a global provider of semiconductor assembly and test services for many of the world’s most successful electronics companies. Unisem offers an integrated suite of packaging and test services such as wafer bumping, wafer probing, wafer gridding, a wide range of leadframe and substrate IC packaging, wafer level CSP and RF, analog, digital and mixed-signal test services. Our turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization. With approximately 7,700 employees worldwide, Unisem has factory locations in Ipoh, Malaysia; Chengdu, People’s Republic of China and Batam, Indonesia. The company is headquartered in Kuala Lumpur, Malaysia.

Yield Engineering Systems (YES) provides a wide variety of processing equipment including vacuum cure systems for polymers and dielectric films. YES manufactures quality equipment for Fan-Out Wafer Level and Panel Level Packaging, Semiconductor, MEMS, Biotech/Life Sciences, and other emerging applications.

Applications for our vacuum cure systems include polyimide/PBO cure, BCB bake for adhesive wafer bonding, low temp polymer cure for temperature sensitive devices, and anneal/drying to improve electrical properties of the different layers.

Our manual and automated vacuum cure systems accommodate up to 300mm wafers and offer critical improvements in any cure process including complete removal of residual solvents, uniform temperature distribution, pressure control, ability to maintain dry inert atmosphere, and control of heating and cooling rates. In addition, YES systems achieve excellent particle performance in most applications.

YES equipment is engineered, manufactured and tested in Livermore, California USA. The answer is YES to quality, flexibility, productivity, and service.

Founded in 1998, Yole Développement (Yole) has grown to become a group of companies providing marketing, technology and strategy consulting, media and corporate finance services, reverse engineering and reverse costing services and well as IP and patent analysis. With a strong focus on emerging applications using silicon and/or micro manufacturing, the Yole group of companies has expanded to include more than 80 collaborators worldwide covering MEMS and image sensors, Compound Semiconductors, RF Electronics, Solid-state lighting, Displays, Software, Optoelectronics, Microfluidics & Medical, Advanced Packaging, Manufacturing, Nanomaterials, Power Electronics, Batteries & Energy Management and Memory. The “More than Moore” market research, technology and strategy consulting company Yole Développement, along with its partners System Plus Consulting, PiSEO, KnowMade and Blumorpho, support industrial companies, investors and R&D organizations worldwide to help them understand markets and follow technology trends to grow their business. For more information, visit www.yole.fr and follow Yole on LinkedIn and Twitter.
Vacuum Cure of Polymers for Advanced Packaging

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www.yieldengineering.com
1.888.YES.3637

Yield Engineering Systems, Inc
Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company’s extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken’s transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company’s people—the foundation of Zuken’s success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken’s people relate to and understand each company’s unique requirements.

Zymet, Inc.
East Hanover, NJ USA
www.zymet.com

Adhesives and encapsulants for electronics and optoelectronics assembly. Products include reworkable and non-reworkable underfill encapsulants, edgefill adhesives, and edgebond adhesives for high reliability board level assembly. Products also include electrically conductive and thermally conductive adhesives, ultralow stress adhesives, ACP’s and NCP’s, and UV curable encapsulants.
# Professional Development Courses (PDCs)

**MONDAY, MARCH 4, 2019**

<table>
<thead>
<tr>
<th>Time</th>
<th>REGISTRATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:00 am – 7:00 pm</td>
<td></td>
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</tbody>
</table>

## PDC Tracks / Themes:

<table>
<thead>
<tr>
<th>Fan-Out PDCs</th>
<th>Heterogenous Integration PDCs</th>
<th>Production / Assembly PDCs</th>
<th>Materials, MEMs &amp; 5G PDCs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MORNING</strong> Professional Development Courses (PDCs) – 10:00am-12:00pm</td>
<td><strong>EARLY AFTERNOON</strong> Professional Development Courses (PDCs) – 1:00pm-3:00pm</td>
<td><strong>LATE AFTERNOON</strong> Professional Development Courses (PDCs) – 3:30pm-5:30pm</td>
<td></td>
</tr>
<tr>
<td>10:00 am – 12:00 pm 2-HOUR FORMAT</td>
<td>1:00 pm – 3:00 pm 2-HOUR FORMAT</td>
<td>3:30 pm – 5:30 pm 2-HOUR FORMAT</td>
<td>5:30 pm – 7:30 pm 2-HOUR FORMAT</td>
</tr>
</tbody>
</table>

### 10:00 am – 12:00 pm 2-HOUR FORMAT

<table>
<thead>
<tr>
<th>PDC1: ROOM 103</th>
<th>PDC2: ROOM 104</th>
<th>PDC3: ROOM 105</th>
<th>PDC4:</th>
</tr>
</thead>
</table>
| Introduction to Fan-Out Packaging
  Course Leader: John Hunt, ASE Group | Introduction to System in Package (SiP) - The Heterogeneous Integration Driver
  Course Leaders: Mark Gerber, ASE Group | Flip Chip Package Technology and Assembly Processes
  Course Leader: Tom Dory, Fujifilm Electronics Materials | Polymers Used in Wafer Level Packaging
  CANCELLED |

### 12:00 pm – 1:00 pm LUNCH

*Only provided for those attendees registered for BOTH Morning and Afternoon PDCs*

### 1:00 pm – 3:00 pm 2-HOUR FORMAT

<table>
<thead>
<tr>
<th>PDC5: ROOM 103</th>
<th>PDC6: ROOM 104</th>
<th>PDC7: ROOM 105</th>
<th>PDC8:</th>
</tr>
</thead>
</table>
| Advances in Fan-Out Wafer Level Packaging (FOWLP)
  Course Leader: Beth Keser, Intel Corporation | Fundamentals of 3D and 2.5D Packaging Integration
  Course Leader: Urmi Ray | Introduction to Solder Flip Chip with an Emphasis on Cu Pillar
  Course Leader: Mark Gerber, ASE Group | MEMS and nanoMEMS Packaging
  CANCELLED |

### 3:00 pm – 3:30 pm COFFEE BREAK IN FOYER

### 3:30 pm – 5:30 pm 2-HOUR FORMAT

<table>
<thead>
<tr>
<th>PDC9: ROOM 103</th>
<th>PDC10: ROOM 104</th>
<th>PDC11: ROOM 105</th>
<th>PDC12: ROOM 106</th>
</tr>
</thead>
</table>
| Fan-Out Wafer/Panel-Level Packaging and 3D IC Heterogeneous Integration
  Course Leader: John Lau, ASM Pacific Technology | Advanced Microelectronics Packaging
  Course Leader: Phil Garrou, Microelectronic Consultants of NC | Introduction to Failure Analysis in Semiconductor Package Assembly
  Course Leader: Tom Dory, Fujifilm Electronics Materials | 5G/mmWave Package Development Requirements and Solutions
  Course Leader: Urmi Ray |

### 5:30 pm – 7:30 pm WELCOME RECEPTION (All Attendees are invited to attend)

**Thank You to the Premier Sponsors:**

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- **JCE**
- **XYZTEC**
- **Namics**
- **Mentor Graphics**
- **Amkor Technology**
- **Emulator Performance Materials**
- **Xperi**
KEYNOTE 1: Sensor Integration: Feynman or Moore?

Sensors are all around us: they are in cars, smartphones, in factories, in pacemakers, in drones, in smart speakers and in many other places with the ultimate goal to sense and to monitor parameters of importance and interest in our daily environment. They play an essential bridge between electronic systems and the user or environment. Today they already enable a multibillion dollar industry and they continue to create new business opportunities in many markets, such as automotive, consumer and personal electronics. Most importantly they are the enablers of emerging applications in Healthcare Industry and Industrial Internet of Things. There is no doubt that sensors will leave a sign in the new generation of home and factory robots, the autonomous cars, enabled by Artificial Intelligence. Thanks to their high reliability, high performances and low manufacturing cost, the most commercially successful sensors available today are realized in silicon (i.e. Image Sensors and MEMS) and they use the same manufacturing techniques of the CMOS industry, whose evolution has been dictated by the famous G. Moore’s law. Since the market for silicon sensors has been much smaller than overall semiconductor industry, sensors have been always classified as part of the so called “More than Moore” world. There are many books, article and publications on “More than Moore” subject, but considering the strong contribution to the sector given by the visionary Nobel Prize P. R. Feynman, envisioning the possibility to miniaturize the microsystems and to stack specialized silicon wafers to realize a complex versatile microsystem, time is come to see the Sensors as part of the “Feynman Roadmap” instead of “More than Moore” roadmap. After an extensive look-back over the current situation, this talk will address the future challenges of “Feynman Roadmap.”

Benedetto Vigna, STMicroelectronics - President, Analog, MEMS and Sensors Group

Benedetto Vigna is STMicroelectronics President, Analog, MEMS and Sensors Group, and has held this position since January 2016. He is a member of ST’s Executive Committee since May 31st, 2016. Vigna joined ST in 1995 and launched the Company’s efforts in MEMS. Under his guidance, ST’s MEMS sensors established the Company’s leadership with large OEMs in motion-activated user interfaces. Vigna has piloted ST’s successful moves into microphones, e-compasses, and touch-screen controllers, as well as environmental sensors, micro-actuators, industrial and automotive sensors, and low-power radars for IoT. Vigna’s mandate was further expanded with analog ICs and RF products (2011) and smart-power devices for OEMs and mass market (2016). ST’s imaging division moved under his management in the fourth quarter of 2017. Vigna has more than 200 patents on micromachining, authored numerous publications, and sits on the boards of several EU-funded programs. Benedetto Vigna was born in Potenza, Italy, in 1969, and graduated with a degree in Subnuclear Physics from the University of Pisa, Italy.

KEYNOTE 2: Life Reimagined: Technology and Business Innovations Driving an Autonomous World

The past few years have seen momentous changes in the automotive industry in areas such as predictive safety, infotainment and hybrid/electric technologies. As the industry gathers pace towards a world of driverless cars, the new norm in technological advances are not only in traditional domains such as power, braking etc. but also in mobile, home, office electronics and their applications to the automobiles we drive. Advanced driver assist systems, electrification and seamless connectivity to our devices near and far are the dominant trends driving the integration of highly innovative electronics in cars. This presentation will discuss how these technologies merge to serve the pilots of these advanced machines and the unique challenges that unifying these diverse domains provide. Innovations in advanced packaging platforms as well as traditional packaging platforms needed to power the electronic content underpinning the autonomous driving world will be discussed in the context of meeting new reliability, vehicle and functional safety as well as security requirements. NXP Semiconductors, as the #1 Global Automotive supplier, is ideally poised to understand the needs of the automotive market and produce innovations in collaboration with partners and suppliers. In addition to discussing the challenges, some of the unique solutions that NXP offers will also be presented as solution examples.

Dr. Veer Dhandapani, NXP Semiconductors – Senior Director, Automotive Package Innovation

Veer Dhandapani is the Head of Automotive packaging at NXP Semiconductors and a Materials Scientist. He is currently responsible for new product and packaging technology development for NXP’s $3.5B Automotive business. In this role, he oversees innovations in leaded and leadless packaging for Microprocessor, Analog, Sensor and Infotainment platforms. He brings 20 years of semiconductor industry experience across multiple strategic, supply chain and technology domains while at Philips Semiconductors, Motorola, Freescale and NXP. Veer Dhandapani has a Bachelor’s degree in Materials Engineering from the Indian Institute of Technology (IIT), Madras, India and a Ph.D. in Materials Science from the University of Cincinnati, OH.
<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker and Details</th>
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</thead>
<tbody>
<tr>
<td>10:30am-11:00am</td>
<td>TA1: 3D IC: Overview of Industry Status</td>
<td>Vinayak Pandey, JCT Group</td>
</tr>
<tr>
<td></td>
<td>TA2: Cost Comparison of Panel Level and Wafer Level Fan-out Packaging</td>
<td>Amy Lujan, SavanSys Solutions LLC</td>
</tr>
<tr>
<td>11:00am-11:30am</td>
<td>TA3: MACROECONOMICS OF AUTOMOTIVE PACKAGING MARKET</td>
<td>Santosh Kumar, Amkor Technology; Tu-Anh Tran, NXP</td>
</tr>
<tr>
<td>10:30am-11:00am</td>
<td>2019dpc065 3D IC: Overview of Industry Status</td>
<td>Vinayak Pandey, JCT Group</td>
</tr>
<tr>
<td></td>
<td>2019dpc001 Cost Comparison of Panel Level and Wafer Level Fan-out Packaging</td>
<td>Amy Lujan, SavanSys Solutions LLC</td>
</tr>
<tr>
<td>11:00am-11:30am</td>
<td>2019dpc061 Advanced Barrier and Seed Layer Deposition Enabling Multiple Type of TSVs Integration</td>
<td>Thierry Mourier, CEA-LETI (Mathilde Gottardi, Pierre-Emile Philip, Sophie Verrun, CEA-LETI; Gilles Romero, STMicroelectronics; Gaelle Guittet, Celine Doussot, Vincent Mevelle; Aveni)</td>
</tr>
<tr>
<td>11:30am-12:00pm</td>
<td>2019dpc028 Processing Through Glass Via (TGV) Interposers</td>
<td>Charles Woychik, i3 Electronics, Inc. (John Lauffer, Michael Gaige, William Wilson, James Carey, Matthew Neely, i3 Electronics, Inc.; Scott Pollard, Raj Parmar, Corning)</td>
</tr>
<tr>
<td>12:00pm-12:30pm</td>
<td>2019dpc011 Through Glass Vias for hermetically sealed High Frequency Application</td>
<td>Kevin Kohnert, Fraunhofer IZM (M. Wöhmann, N. Jürgensen, K.D. Lang, T. Galler, T. Chaloun, C. Waldschmidt, M. Schulz-Ruhenberg, N. Ambrosius, R. Oštolt)</td>
</tr>
<tr>
<td>12:30pm-2:00pm</td>
<td>Lunch Break in the Exhibit Hall Sponsored by:</td>
<td>(food served 12:30pm - 1:30pm)</td>
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</tbody>
</table>

The image contains an advertisement for Golden Altos, including their mission statement and website.
# TUESDAY, MARCH 5, 2019

## Afternoon Technical Sessions

<table>
<thead>
<tr>
<th>TUESDAY AFTERNOON SESSIONS:</th>
<th>DUAL TRACK: Automotive Packaging</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>APPLICATIONS &amp; PROCESSES</strong></td>
<td><strong>DIVERSE AUTOMOTIVE PACKAGING TECHNOLOGIES</strong></td>
</tr>
<tr>
<td>Chairs: Dongshun Bai, Brewer Science; Rafiql Islam, Cactus Materials</td>
<td>Chairs: Mark Gerber, ASE US; Linda Bal, TechSearch International</td>
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<tr>
<th>2:00pm-2:30pm</th>
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<tbody>
<tr>
<td>2019dpc055 High-Performance, Heterogeneous IC Packaging Trends</td>
<td>2019dpc016 Ultra-low Warpage and Anhydride-free Liquid Compression Molding Techniques for Advanced Semiconductor Packaging</td>
<td>2019dpc013 Copper Ball Voids: Failure Mechanisms and Methods of Controlling at High Temperature Automotive Application</td>
</tr>
<tr>
<td>Mike Kelly, Amkor Technology Inc. (Curtis Zwenger, Ron Huemoeller)</td>
<td>Tim Champagne, Henkel Electronic Materials (Jay Chao, Kazuyasu Tanaka, Ramachandran Trichur, Rong Zhang)</td>
<td>Chu-Chung Lee, NXP Semiconductor Inc. (TuAnh-Tran, Varughese Mathew, Rusli Ibrahim, Poh-Leng Eu)</td>
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<tbody>
<tr>
<td>William Vis, SUSS MicroTec Photonic Systems Inc. (Fabian Benthaus, Habib Hichri, Markus Arendt)</td>
<td>Nokibul Islam, JCET Group (KH Tan, Tony Chen)</td>
<td>Kuldip Johal, Atotech GmbH (Rick Nichols, Sandra Nelle, Gustavo Ramos, Atotech GmbH; David Unruh, Intel Corp.)</td>
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<tr>
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<tbody>
<tr>
<td>Jennifer Kitchen, Arizona State University (Soroush Moallemi, Sumit Bhardwaj)</td>
<td>Stefan Kempa, Atotech GmbH (Wolfgang Friz, Florian Gaul, Ellen Habig, Laurence Gregoriades, Roger Massey)</td>
<td>John Moore, Daetec LLC (Jevon Spencer)</td>
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</tbody>
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<tbody>
<tr>
<td>Rafiql Islam, Cactus Materials, Inc. (Ajit Dhamdhere, Wey Lyn Lee)</td>
<td>Sherman Peak, Auburn University (Vaibhav Gupta, Bhargav Yelamanchili, Thomas Stegeman, Tamara Isaacs-Smith, John Sellers, David Tuckerman, Michael Hamilton)</td>
<td>Rajesh Tripathi, DuPont (Sejin Im, Douglas Devoto, Joshua Major, Sreekant Narumanchi, Paul Paret, Xuhui Feng)</td>
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<tbody>
<tr>
<td>Kevin Moody, ACCESS Technologies, USA (Nick Stukan)</td>
<td>Hiroshi Komatsu, CONNECTEC JAPAN Corp. (Hidekazu Machida, Nozomi Shimoisihikawa)</td>
<td>Gerald Weis, AT&amp;S Austria Technologie und Systemtechnik Aktiengesellschaft</td>
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<tr>
<td>Chairs: Dongshun Bai, Brewer Science; Rafiql Islam, Cactus Materials</td>
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<td>Kevin Moody, ACCESS Technologies, USA (Nick Stukan)</td>
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<thead>
<tr>
<th>6:30pm-8:30pm</th>
<th>EVENING KEYNOTE &amp; PANEL DISCUSSION</th>
<th>EVENING KEYNOTE &amp; PANEL DISCUSSION</th>
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</thead>
<tbody>
<tr>
<td>Chairs: Dongshun Bai, Brewer Science; Rafiql Islam, Cactus Materials</td>
<td>Details on the following page</td>
<td>Details on the following page</td>
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</tbody>
</table>

### Break in the Exhibit Hall Sponsored by: METALOR

### Exhibit Hall Reception Sponsored by: MacDermid Alpha, TECHNIC, JX Nippon Mining & Metals
6:30pm-8:30pm

Panel Session & Refreshments Sponsored by:

EVENING KEYNOTE & PANEL DISCUSSION  (ROOM 107-108)

Panel Session & Refreshments Sponsored by:

KEYNOTE 3: Directions in Advanced Packaging Technology
This talk will address the role of packaging in enabling Heterogeneous Integration and will focus primarily on the technology evolution of package interconnect densities & future challenges in interconnect density scaling.

Sriram Srinivasan, Intel Corporation – Principal Engineer
Sriram Srinivasan is a Principal Engineer with Intel Corporation responsible for package architecture and technology definition for Intel products. He has been with Intel-Packaging for 18 years. His focus is on Silicon-package-platform co-design to deliver optimized product and technology. He has numerous patents in the areas of package design, assembly process and interconnect technologies. Sriram holds a Master’s in Chemical Engineering from University of Kansas.

PANEL DISCUSSION ON:
Heterogenous Integration: Why Now?
The discussion will focus on the drivers for heterogeneous integration and types of advanced packages being introduced today and in the future. Challenges and issues for these packaging solutions will be discussed.

MODERATOR:
E. Jan Vardaman, TechSearch International, Inc.

PANELISTS:
Bill Chen, ASE
Nokibul Islam, JCET Group
Mike Kelly, Amkor Technology
Dan Oh, Samsung Electronics
Rajendra (Raj) Pendse, Facebook Reality Labs
Sriram Srinivasan, Intel Corporation

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## Welcome to the Global Business Council (GBC) Keynote & Plenary Session on

**TRANSFORMING POWER PACKAGING**

(Room 107-108)

### Registration

7:00am-6:00pm

### Continental Breakfast Sponsored by:

<table>
<thead>
<tr>
<th>Company</th>
<th>Logo</th>
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<tbody>
<tr>
<td>EMD Performance Materials</td>
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<tr>
<td>XYZTEC</td>
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<tr>
<td>JCET</td>
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</table>

### GBC Opening Comments

**GBC Chairs:** Lee Smith, (UTAC) United Test & Assembly Center; Rich Rice, ASE USA, Inc.; Thomas Goodman, Izinus

### GBC Keynote: Cars and Clouds: New Drivers for Efficient Power Management

**Dr. Hans Stork, ON Semiconductor – Senior Vice President and CTO**

Dr. Hans Stork is Senior Vice President and Chief Technology Officer (CTO) at ON Semiconductor. He oversees the development of wafer process technologies, modeling and design kits, design libraries, as well as packaging technologies and assembly support.

Prior to joining ON Semiconductor, Dr. Stork was Group Vice President and CTO of the Silicon Systems Group at Applied Materials. From 2001 to 2007 he was Senior Vice President and the CTO of Texas Instruments. Before that, Dr. Stork held various R&D and management positions at Hewlett Packard Laboratories and at IBM’s T.J. Watson Research Center.

Dr. Stork was born in Soest, The Netherlands, and received the Ingenieur degree in electrical engineering (EE) from Delft University of Technology, Delft, The Netherlands, and holds a PhD in EE from Stanford University.

### Packaging Trends and Challenges for Power Devices

**E. Jan Vardaman, TechSearch International, Inc.**

Power devices are experiencing strong growth driven by demand in a variety of areas. Applications including energy generation and infrastructure, electric and hybrid vehicles, electric vehicle charging, datacenters, industrial automation, smart cities and buildings, home appliances, and transportation are driving demand for power devices. While many companies continue to expand production of silicon-based power devices, there is also demand for devices based on new wide bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN). Driven by the need for increased power density and system efficiency, these WBG materials are being adopted in many applications and may require new packages, materials, and assembly methods. This presentation describes package trends and discusses some of the challenges faced.

### Modern Cell Phone Power Electronics Overview and Future Challenges

**Todd Sutton, Qualcomm**

The second largest thing in your cell phone is the battery and roughly half of the electronics is associated with power management. This talk will provide an overview of these systems and shed some light on the challenges in the not so distant away future.

### Break in the Exhibit Hall

(Wasaja Ballroom)

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**JOIN US FOR DEVICE PACKAGING 2020**

*Look for Details at Registration! March 2-5, 2020.*
<table>
<thead>
<tr>
<th>Time</th>
<th>Event</th>
</tr>
</thead>
</table>
| 10:45am-11:15am | **Power Module Packaging: Market & Technology Trends**  
Elena Barbarini, SystemPlus Consulting; Claire Troadec, Yole Développement  
In recent years, several new power module designs have emerged, principally driven by the severely challenging requirements for high power density and integration from the automotive industry. Indeed, electric and hybrid cars are the best example of technology innovation in the design of power modules. The Toyota Prius’ fourth generation double-sided cooling power modules might be the most well-known example. Yet today many other module manufacturers are also proposing new designs that move away from conventional power module layers and technologies. In our presentation, we will start with market trends and illustrate how industrial applications still remain the biggest part of the power module market. We will then demonstrate that the automotive industry is leading in technological innovations in packaging, helping and accelerating the implementation of these new technologies thanks to high manufacturing volumes. We will detail these technology trends by providing real teardown and cost analysis of various power modules. We will explain how they are creating opportunities for some material suppliers, and at the same time, are transforming today’s businesses for power packaging. |
| 11:15am-11:45am | **IC Market Update and China Impact Analysis**  
Bill McClean, IC Insights  
A high level of uncertainty looms over the global economy and sales of smartphones are beginning to saturate. However, the Internet of Things, driver assisted autos, and AI hold promise for the future. In order to make sense out of the current turmoil, a top-down analysis of the IC market will be given and include trends in worldwide GDP growth, electronic system sales, and semiconductor industry capital spending. A critical look at China’s ambitions to become a bigger player in the IC industry will also be presented. |
| 11:45am-12:00pm | **GBC CLOSING REMARKS** |
| 12:00pm-1:30pm | **Lunch Break in the Exhibit Hall Sponsored by:** (food served 12:00pm - 1:00pm)  
ASE GROUP |

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**Electroless Bumping**
- Electroless Ni/Au & Ni/Pd/Au UBM/OPM  
- No tooling  
- 4 - 12“ Wafers  
- Up to 150 Wafers/hour  
- In-line bathcontrol

**Laser Solder Jetting**
- Fluxless Solder Jetting  
- Deballing & Rework  
- BGAs, Single Chips  
- Wafers up to 12“  
- 3D Soldering  
- MEMS

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<table>
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<tr>
<th>Time</th>
<th>Session</th>
<th>Title</th>
<th>Speaker(s)</th>
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<tbody>
<tr>
<td>1:30pm-2:00pm</td>
<td>2019dpc060, 2019dpc027, 2019dpc008</td>
<td>What is Driving the TSV Business: Market &amp; Technology Trends</td>
<td>Santosh Kumar, Yole Developpement, Diane Peng, Quantenna Communication (Baqar Tabrez), Fu Xi Zhang, Auburn University (George Flowers, Edmon Perkins, Robert Dean, Jeffrey Suhling, Jordan Roberts)</td>
</tr>
<tr>
<td>2:00pm-2:30pm</td>
<td>2019dpc005, 2019dpc019, 2019dpc023</td>
<td>The Bifurcation of Advanced IC Packaging</td>
<td>John Park, Cadence Design Systems, Tunir Dey, Zukan, Inc. (Kazunari Koga, Humair Mandavia), Arthur Bond, Auburn University (Brent Bottenfield, Mark Adams, Robert Dean)</td>
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<tr>
<td>2:30pm-3:00pm</td>
<td>2019dpc015, 2019dpc038, 2019dpc035</td>
<td>Post-layout Electrical Analysis for High-density Advanced Packaging</td>
<td>Tarek Ramadan, Mentor a Siemens Business (Dusan Petranovic), Stefan Kempa, Atotech GmbH (Christian Wendelin, Edith Steinhauser, Lutz Stamp, Bexy Dosse-Gomez, Elisa Langhammer, Sebastian Reiber, Sebastian Duenneboll, Sandra Roeseler, Roger Massey), Kurt Christenson, Optomec</td>
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<tr>
<td>3:00pm-4:00pm</td>
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<td>Break in the Exhibit Hall</td>
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<tr>
<td>4:00pm-4:30pm</td>
<td>2019dpc014, 2019dpc021, 2019dpc036</td>
<td>Automated Daisy Chain Generation and Verification</td>
<td>Tom Whipple, Viasat (Doug Mathews, Viasat; Tom Hoang, Zukan), Brent Bottenfield, Auburn University (Artie Bond, Mark Adams, Robert Dean)</td>
</tr>
<tr>
<td>4:30pm-5:00pm</td>
<td>2019dpc050, 2019dpc035, 2019dpc049</td>
<td>Ceraphene\textsuperscript{TM} - a Stack of CVD Graphene and Ceramic Materials (2D) for Thermal Management of 2.5D/3D Packages</td>
<td>Rifqul Islam, Cactus Materials, Inc. (Ajit Dhamdhere, Wey Lyn Lee), Shengmin Wen, Synaptics Inc. (Jason Goodelle)</td>
</tr>
<tr>
<td>5:00pm-5:30pm</td>
<td>2019dpc046, 2019dpc049, 2019dpc066</td>
<td>Material Design Advancement Create Multifunctional Materials for Single-Layer Temporary Bonding and Debonding, Microbump Processing for 3D IC Integration, Isolated Interposers for MEMS Sensors</td>
<td>Luke Prenger, Brewer Science (Xiao Liu, Qi Wu, Rama Pulligoda), Feng Li, University of Idaho (Qianyi Li, Andrew Owens), Michael Kranz, EngeniusMicro (Michael Whitley, Brian English, Mark Adams, Robert Dean, Brent Bottenfield, Artie Bond)</td>
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</table>
**POSTER SESSION & HAPPY HOUR**
Outside on Patio Overlooking Desert: 5:30 pm - 6:30 pm
(Poster Presenter Setup - 4:00 pm - 5:25 pm)

*Poster Session & Happy Hour Sponsored by:*

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**Session Chair: Syed Sajid Ahmad, ECE, NDSU**

2019dpc002
*Can Electrolytic Capacitors Meet the Demands of High Reliability Applications?*
Greg Caswell, DfR Solutions (Paul Parker)

2019dpc029
*A New Photosensitive Dielectric Material for High-Density RDL with Ultra-Small Photo-Vias and High Reliability*
Daichi Okamoto, Taiyo Ink Mfg. Co. Ltd. (Yoko Shibasaki, Daisuke Shibata, Tadahiko Hanada)

2019dpc030
*High-Throughput Precise Dotting in Electronics Assembly*
Hanzhuang Liang, Nordson Asymtek (Akira Morita, Brian Chung)

2019dpc039
*Advanced Adhesion Promotor System for IC Substrate Packaging*

2019dpc067
*Direct Die-placement Technology for Component Attach in Thin and Lightweight Electronics*
David Grierson, systeMECH, Inc. (Kevin Turner, Wilfried Bair)

2019dpc069
*Optimising Surface Chemistry After Plasma Dicing*
Stewart Fulton, Janet Hopkins, SPTS Technologies Newport (Oliver Ansell, SPTS Technologies Newport; Michael Phenis, Don Plettscher, Richie Peters, Mark Sistem, Versum Materials US, LLC)

2019dpc072
*A Technique for Reducing System Form Factor in Electronic Systems*
Benjamin Rhea, Auburn University (R. Chase Harrison, Robert Dean)

2019dpc074
*Semiconductor Packaging and CDM ESD Risk*
Stevan Hunter, ON Semiconductor (Nicholas Vincetic, Arizona State University)

2019dpc075
*Interfacial Degradation of Copper Wire Bond due to Growth of Cu9Al4 phase*
Stevan Hunter, ON Semiconductor (Subramani Manoharan, Chandradip Patel, Patrick McCluskey, CALCE, University of Maryland)

2019dpc080
*Rapid Dissolving of Dry Film Resist (DFR) Using Green Products*
John Moore, Daetec LLC

2019dpc001
*Cost Comparison of Panel Level and Wafer Level Fan-out Packaging*
Amy Lujan, SavanSys Solutions LLC)

2019dpc035
*Organic Substrate Technologies for Fingerprint Sensors*
Shengmin Wen, Synaptics Inc. (Jason Goodelle)

2019dpc037
*Design, Processes & Technology Co-design Methodology for Advanced Package Assembly in HVM*
Diane Peng, Quantenna Communication (Baqar Tabrez)

2019dpc038
*Impact of Glass Filler Removal on Electroless Copper Performance in Advanced Build-up-films*
Stefan Kempa, Atotech GmbH (Wolfgang Friz, Florian Gaul, Ellen Habig, Laurence Gregoriades, Roger Massey)

2019dpc039
*Novel Formaldehyde-Free Electroless Copper Solution for Next Generation Substrates*
Stefan Kempa, Atotech GmbH (Christian Wendeln, Edith Steinhauser, Lutz Stamp, Bexy Doss-Gomez, Elisa Langhammer, Sebastian Reiber, Sebastian Duennbeil, Sandra Roeseler, Roger Massey)

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**2019 3D InCites Awards Ceremony**

*Hosted by IMAPS*

6:30pm-8:00pm
Immediately Following the Poster Session - Outside On Patio Overlooking Desert

DETAILS ON THE FOLLOWING PAGE
ELECTRONIC MATERIALS

Sputtering Targets
Electroplating Anodes
Compound Semi Wafers

- ITAR-Registered, AS9100D/ISO9001:2015
- DMEA Trusted Foundry - Pending
- WLP: Bumping/Micro-bumping, Cu Pillar, Redistribution
- Wide selection of WLP processes, materials and solder alloys, including high-Pb and Pb-free
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- Flip-Chip and Multi-Chip Module Assembly
- Novel Micro-fabricated devices, including IR sensors
- Monolithic Integration, Vacuum Microelectronics, Wafer-Level Hermetic Packaging
- Column Grid Array (CGA)

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Please join us for an evening of fun, games, and prizes as we celebrate the winners of the 2019 3D InCites Awards and celebrate the 10th Anniversary of 3D InCites with the 3D InCites Awards Ceremony Barbeque on Wednesday, March 6, from 6:00 - 8:00 PM.

• Watch the on-site creation of the 2019 mural. This year's theme is "Celebrating 25 Years of Advanced Packaging Innovation." Donate $500 to own a milestone on the timeline.
• Compete in the Awards Ceremony Quiz during the ceremony and win a prize!
• Capture memories with your friends and colleagues at our photo booth
• Enjoy a fully catered Wrangler barbeque buffet, including beer, wine, and iced tea.

New this year, is the **3D InCites SemiSister™ Award** -- awarded to an individual or company that demonstrates the most gender diversity and inclusion.

The 2019 3D InCites Awards will be presented in the following categories:

* Device of the Year
* Process of the Year
* Device Manufacturer of the Year
* Startup of the Year
* Equipment Supplier of the Year
* Materials Supplier of the Year
* EDA Provider of the Year
* Research Institute of the Year
* Engineer of the Year
* SemiSister of the Year

A portion of the proceeds from the event will benefit two charities: the [IMAPS Microelectronics Foundation](#), which exists to support student activities related to the study of microelectronic packaging, interconnect and assembly; and [Phoenix Children’s Hospital pediatric oncology programs](#), the only institution in Arizona conducting Phase I trials, giving pediatric cancer patients access to the latest and most advanced treatments available.

*(Participation is included in your registration fee, but space is limited.)*
Thursday, March 7, 2019

Morning Technical Sessions

7:00am-11:30am  Registration

7:00am-8:00am  Continental Breakfast Sponsored by:

8:00am-8:45am  Keynote Sessions Sponsored by:  (Room 107-108)

8:45am-9:30am  Keynote 5:

New Directions in Si/Packaging for AR/VR Hardware

Dr. Rajendra (Raj) D. Pendse, Facebook Reality Labs – Silicon/Packaging Architect

The AR/VR hardware of tomorrow is set to carve out a new trajectory in power/performance and form factor quite unlike anything we have seen in the realm of modern-day consumer hardware and rivaled only by the human brain. This will range from logic, memory and sensor devices powered with AI for ultralow power consumption, life-like imaging and display technologies to enable integration in constrained form factors – it will include new 3D stacking architectures, wafer-level packaging, heterogeneous integration, low loss dielectric materials and predictive tools for performance and reliability modeling. We will look at the packaging challenges from a holistic system-package-Si view point and present new approaches and solutions being developed to address the challenges; and finally, a vision of what the future holds in the 5-10-year horizon.

Dr. Rajendra ‘Raj’ D. Pendse joined Facebook Reality Labs in 2017 where he is leading the Silicon and Packaging Research team that develops next-generation silicon and packaging technologies for advanced AR/VR and mixed reality products. Prior to Facebook, Dr. Pendse was the Director of Packaging at Qualcomm where he led a team that enabled the development of high-performance silicon foundry products, for a wide range of applications. He received his Ph.D. in Electrical Engineering from UC Berkeley in 1996, after completing an M.S. in Electrical Engineering from the University of Illinois in 1993. He has held leadership roles in packaging at National Semiconductor, Intel, Rambus, and STATS ChipPAC. Dr. Pendse is an author of over 60 technical papers and holds 34 US patents in the areas of signal integrity, power integrity, interconnect design, and reliability. He is a member of the Technical Council of IEEE EMC and a member of the IEEE Electromagnetics Committee in the Field of Electronics and Photonics. He is a Senior Member of the IEEE and a Distinguished Lecturer of the IEEE EMC Society.

9:30am-9:45am  Break in the Foyer

The DPC 2019 presentations will be ARCHIVED into IMAPS online research portal/library, IMAPSource®, around April 15th.

IMAPSource® currently features all of IMAPS proceedings, journal papers, magazines, and DPC/other conference publications back to 2010. This new portal is a fully searchable, Google Scholar®-friendly database.

Get Searching for DPC files today!
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<th>Time</th>
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<th>Title</th>
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<td>THURSDAY MORNING SESSIONS:</td>
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<tr>
<td>9:45am-10:15am</td>
<td>2019dpc051 Temporary and Permanent Bonding Enables 3D Integration of Ultrathin Wafers</td>
<td>Thomas Uhrmann, EVG (Elisabeth Brandl, Mariana Fires, Stefan Jung, Juergen Burggraf, Matthew Koch)</td>
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<td>2019dpc009 Quick Prototyping Design for More than Moore Era</td>
<td>Yoko Fujita Zuken Inc. (Kazukuni Koga, Zuken Inc.; Shintaro Ohtani, Daisuke TsuTsu, Socionext Inc.)</td>
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<td>2019dpc003</td>
<td>Robert M. Weikle II, University of Virginia (S. Nadri, C.M. Moore, N.D. Sauber, L. Xie, M.E. Cybereny, N. Scott Barker, A.W. Lichtenberger, M Zebarjad)</td>
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<tr>
<td>10:15am-11:15am</td>
<td>2019dpc007 Key Enabling Materials for 3DIC Fabrication and Device Performance</td>
<td>Michael Gallagher, DuPont Electronics and Imaging (Ed Anzures, Robert Auger, Rosemary Bell, Paul, Berry, Hua Dong, Michelle Ho, Joe Lachowski, Yi-Hak Lee, Masaki Kondo, Julia Kozhuhik, Paul Morganelli, Janet Okada, Ravi Pokhrel, Jonathan Prange, Matthew VanHanehlem)</td>
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<td>2019dpc021</td>
<td>Robert Dean, Auburn University (Lauren Beckingham, Michael Bozack)</td>
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<td>2019dpc022 Process Control for Advanced Packaging Metallization</td>
<td>Eugene Shalyt, ECI Technology (Michael Pavlov, Danni Lin, Michael MacEwan, Helen Lu, Paul Okagbare)</td>
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<td>2019dpc045</td>
<td>Li-Anne Liew, National Institute of Standards and Technology &amp; University of Colorado (Ching-Yi Lin, Collin Coolidge, Y.C. Lee)</td>
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<td>11:15am-11:45am</td>
<td>2019dpc068 Dicing Tape Performance in a Plasma Dicing Environment</td>
<td>Stewart Fulton, SPTS Technologies Newport (Oliver Ansell, Janet Hopkins, SPTS Technologies Newport; Taku Umemoto, Takuo Nishida, LINTEC Advanced Technologies (Europe) GmbH)</td>
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<td>2019dpc022</td>
<td>En FOREST Control for Advanced Packaging Metallization (Michael Pavlov, Danni Lin, Michael MacEwan, Helen Lu, Paul Okagbare)</td>
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<td>2019dpc054</td>
<td>Ti-Pd-Au as a Sacrificial Layer, Buried Interconnect and Etch Mask for Fabrication of Polyimide Surface Micromachined Micropumps Li-Anne Liew, National Institute of Standards and Technology &amp; University of Colorado (Ching-Yi Lin, Collin Coolidge, Y.C. Lee)</td>
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**Conference Ends**
FOUNDATION GOLF OUTING AT 1:30PM at WeKoPa Golf Course (Saguaro Course)
SiP 2019 is a continuation of IMAPS SiP Conference which first started in June 2017 as the first System-in-Package (SiP) conference fully dedicated to covering all aspects related to SiPs - market trends, system integration/miniaturization, and new technology innovation enablers to meet current and future SiP challenges.

June 25-27, 2019
Monterey Marriott
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Monterey, California
USA

www.advancedsip.org

For more information about IMAPS and other 2019 events, visit www.imaps.org.

The 52nd International Symposium on Microelectronics is organized by the International Microelectronics Assembly and Packaging Society (IMAPS).

September 30 - October 3, 2019
Boston, Massachusetts

• Returning to favored Boston for the first time in over a decade, with local activities and networking events
• Over 125 papers across 5 tracks, plus the ever-popular interactive poster session
• 16 Professional Development Courses
• Two days of exhibits featuring the newest and best technologies in the microelectronics supply chain

More information available at
www.imaps2019.org
More technical papers, keynotes, and coverage of FOWLP, 3D, Automotive, and Micro Systems than any other competing Conference!

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- “Call For Abstracts” begins NEXT MONTH - submit early - space is limited
- Sponsor & Exhibit “Presale” in JUNE
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