IMAPS 12th International Conference and Exhibition on Device Packaging

March 14 - 17, 2016
WeKoPa Resort and Casino
Fountain Hills, Arizona - USA

Interposers, 2.5/3D IC & Packaging

Fan-Out, Wafer Level Packaging, Flip Chip

SiP & Engineered Micro Systems/Devices (MEMS & Sensors)

Monday, March 14
8 Professional Development Courses & Welcome Reception

Tuesday, March 15 - Thursday, March 17
14 Technical Sessions | 4 Keynotes | 80+ Speakers
Exhibit Hall Reception (Tuesday 5:00 pm - 6:30 pm)
PANEL: SiP: New Drivers and the Supply Chain (Tuesday 6:30 pm)

Wednesday, March 16
Global Business Council Plenary Session & Keynote
Poster Session & “Happy Hour” (5:30 pm - 6:30 pm)

Thursday, March 17
Foundation Spring Golf Invitational: 1:00 pm Tee Off

Exhibition
Sold Out Exhibit Hall!

Tuesday, March 15
10:00 am - 6:30 pm

Wednesday, March 16
10:00 am - 4:00 pm

General Chair:
Rozalia Beica, Yole Developpement

General Chair-Elect:
Peter Ramm, Fraunhofer EMFT

Past General Chair:
Ron Huemoeller, Amkor Technology

Technical Chairs:
Jeff Calvert, Dow Electronic Materials (3D)
Kathy Cook, Ziptronix (3D)
Rahul Agarwal, GlobalFoundries (3D)
Jon Aday, Qualcomm (FC/FO-WLP)
John Hunt, ASE US (FC/FO-WLP)
Robert Dean, Auburn University (Eng. Micro Sys.)
Russell Shumway, Amkor Technology (Eng. Micro Sys.)
Nozad Karim, Amkor Technology (SiP)

Hotel Cut-off: February 10, 2016
Early Registration & Exhibit Deadlines: February 10, 2016

Advance Program and Registration on-line: www.imaps.org/devicepackaging

DPC/GBC Premier Sponsors:

Amkor Technology
NAMICs

Exhibition

ASE GROUP

Organized by: International Microelectronics Assembly and Packaging Society (IMAPS)
Bringing Together the Entire Microelectronics Supply Chain!
Innovative IC, System-in-Package, and MEMS packaging portfolio for today’s miniaturization, mobility, and IoT needs.
The 12th Annual Device Packaging Conference (DPC) will be held in Fountain Hills, Arizona, on March 14-17, 2016. It is an international event organized by the International Microelectronics Assembly and Packaging Society (IMAPS). IMAPS International Device Packaging Conference is one of the premier conferences held each year where the latest in packaging technology and trends is unveiled. The DPC provides the stage to showcase the best in packaging technology available today as well as those technologies soon to be released to the market. It offers the benefit of technical exchange among key international players and the opportunity to discover key business trends from internationally-known marketing analysts.

The conference provides a focused forum on the latest technological developments in 3 topical workshop tracks related to microelectronic packaging: Interposers, 3D IC & Packaging; Flip Chip, Wafer Level Packaging & FAN-OUT; and SiP & Engineered Micro Systems/Devices (including MEMS & Sensors). The 2016 conference will feature:

- 4 premier Keynote speakers;
- Global Business Council (GBC) keynote and plenary session on the System Integration and Package Assembly Supply Chain Implications on Wednesday morning;
- NEW Panel Discussion on SiP: New Drivers and the Supply Chain on Tuesday evening;
- 14 technical sessions featuring more than 80 technical presentations;
- the interactive poster session “happy hour”;
- 8 professional development courses (Monday);
- a sold-out vendor exhibition and technology showcase;
- and more, all covering the latest in packaging technology innovation.

There will be several networking receptions and gatherings throughout the week, including: the welcome reception (Monday); the exhibit hall reception (Tuesday); the Poster Session and “Happy Hour” Wednesday; a charity “Texas Hold 'em” Tournament (Monday); a charity golf outing (Thursday); and other social events.

We hope to see you this March in sunny Arizona!
Customer demand for highly sophisticated products has made semiconductor packaging an important factor in system performance. As one of the world’s largest suppliers of outsourced semiconductor packaging design, assembly and test services, Amkor helps make “next generation” products a reality.

Founded in 1968, Amkor’s continuous path of innovation, improvement and growth has led us to be a strategic and trusted manufacturing partner for many of the world’s leading semiconductor companies. As the industry moves aggressively toward new and more complex technologies, our unique expertise in high-volume manufacturing techniques and the ability to solve technological challenges are among our greatest strengths.

Customers also benefit from our extensive and expanding global footprint, enabling us to easily handle large orders and offer quick turnaround times. Amkor is positioned to deliver end-to-end solutions that meet the requirements for a broad range of product designs today, and in the future.

www.amkor.com
Program at a Glance

Monday, March 14
Registration and Continental Breakfast: 7:00 am - 8:00 am
Professional Development Courses (PDCs): 8:00 am - 5:00 pm

Professional Development Courses (PDC) - FULL DAY: 8:00 am - 5:00 pm
PDC1
MEMS and the Internet of Things: Principles, Applications, Power Supplies and Device Packaging  (8-hour)
Course Leader: Slobodan Petrovic, Oregon Institute of Technology

Professional Development Courses (PDC) - 1/2 Day: 8:00 am - Noon
PDC2
Introduction to Microelectronics Packaging (Part 1)
Course Leader: Tom Green, TJ Green & Associates

PDC3
Introduction to Fan-Out Wafer Level Packaging (FO-WLP)
Course Leader: Beth Keser, Qualcomm Technologies, Inc.

PDC4
New
Electrical Modeling and Test Strategies for 3D Packages
Course Leader: Bruce Kim, City University of New York

Professional Development Courses (PDC) - 1/2 Day: 1:00 pm - 5:00 pm
PDC5
Performance based Roadmaps for Advanced Packaging
Course Leader: Dev Gupta, APSTL

PDC6
Introduction to Microelectronics Packaging (Part 2)
Course Leader: Tom Green, TJ Green & Associates

PDC7
Emerging Challenges in Packaging
Course Leader: Raja Swaminathan, Intel Corporation

PDC8
Polymers for Electronic Packaging
Course Leader: Jeffrey Gotro, InnoCentrix, LLC

Welcome Reception: 5:00 pm - 7:00 pm

2016 Texas Hold’em Tournament: 7:00 pm - 10:00 pm
To Benefit the IMAPS Microelectronics Foundation

Tuesday, March 15
7:00 am - 7:00 pm
Registration
8:20 am - 9:55 am
Keynote Presentations
10:00 am - 6:30 pm
Exhibits Open
10:30 am - 12:30 pm
Morning Technical Session
12:30 pm - 2:00 pm
Lunch Break In Exhibit Hall
(Food served from 12:30 pm - 1:30 pm)
2:00 pm - 5:30 pm
Afternoon Technical Sessions
5:00 pm - 6:30 pm
Reception In Exhibit Hall
6:30 pm - 8:00 pm
New Evening Panel:
SIP: New Drivers and the Supply Chain
GBC Speaker Dinner (by Invitation):
8:00 pm

Wednesday, March 16
7:00 am - 6:00 pm
Registration
8:00 am - 12:00 pm
GBC Keynote & Plenary Session on System Integration and Package Assembly Supply Chain Implications
10:00 am - 4:00 pm
Exhibits Open
12:00 pm - 1:30 pm
Lunch Break In Exhibit Hall
1:30 pm - 5:30 pm
Afternoon Technical Sessions
5:30 pm - 6:30 pm
Poster Session & “Happy Hour” Outside on Patio/Grass
(Will move inside if weather issues)
(Poster setup: 4:00 pm - 5:00 pm)

Thursday, March 17
7:00 am - 11:00 am
Registration
8:00 am - 9:30 am
Keynote Presentations
9:45 am - 11:45 am
Morning Technical Sessions
11:45 am
Closing Remarks
1:00 pm - 7:00 pm
IMAPS Microelectronics Foundation Spring Golf Invitational (Separate Registration)
SunRidge Canyon Golf Club
1:00 pm Shotgun Start
“Best Ball” Scramble Details enclosed and online.
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The broad areas that the IoT will encompass are environmental monitoring and control, infrastructure management, manufacturing, energy management, transportation, and other large scale deployments. All these devices will create a cluster connecting them to the Internet. The systems will also perform actions and MEMS actuators will provide control and actuation capabilities over the "things" or objects.

MEMS or nanoMEMS sensors. These sensors, electronics and software are part of the network of physical objects or "things." In principle, MEMS or nanoMEMS sensors detect the physical world, e.g., temperature, pressure, motion, sound, humidity, or chemical and biological inputs, and wirelessly processed and appropriate action is taken. The IoT is a major opportunity for MEMS. Billions of MEMS and nanoMEMS devices will be in the heart of this communication revolution that has already started and which value is expected to reach US$1 trillion by the end of the decade.

Who Should Attend?
The course is open to anyone with general understanding of the physics, chemistry, and material science. The participants will have the opportunity to explore highly speculative, futuristic concepts and develop visionary views of the technological possibilities using micro and nano technology in the revolutionary concept of the Internet of Things. The course is open to participants with no prior MEMS, nantotechnology, or power sources knowledge and would provide a reasonably broad general introduction into all three areas of technology.

Dr. Slobodan Petrovic is an associate professor at the Oregon Institute of Technology in Portland, OR. His research interests are in the areas of MEMS fuel cells, sensor media compatibility, hydrogen generation and storage, and dye-sensitized solar cells. Prior to that, he was at the Arizona State University, where he taught courses in MEMS, Sensors, and alternative energy. Dr. Petrovic also held appointments at Clear Edge Power as a Vice President of Engineering; at Neah Power Systems as Director of Systems Integration; and Motorola, Inc. as a Reliability Manager. Dr. Petrovic has over 25 years of experience in MEMS, sensors, energy systems; fuel cells and batteries; and electrochemical solar cells. He has over 50 journal publications and conference proceedings; 2 book contributions and 24 pending or issued patents.
PDC2: Introduction to Microelectronics Packaging (PART I)
Course Leader: Thomas Green, TJ Green Associates LLC
Morning PDC: 8:00am – 12:00pm | $400 (Through 2/10/2016) - $450 (after 2/10/2016)

Course Description:
Introduction and Overview of Microelectronic Packaging

- What is microelectronic packaging
  - What are we trying to package and why?
- Packaging drivers
  - Cost, Size, Weight, Thermal
- Market segments
  - Commercial, Automotive, Medical, Aerospace etc.
- Terminology and product definitions
- Includes pass around of sample packages
- Who are the players?
- How does the supply chain work
- Basic review of IC Fab processes
- Wafer sawing and thinning
- Substrates
  - HDI laminates, LTCC/HTCC, Flex, Teflon and RF board material
- Fundamentals of component attach
  - Epoxy adhesives and eutectic solders
- Wirebonding Interconnect technology
  - Gold and copper ball bonding, wedge bonding
- Flip chip assembly processes
- Transfer molding of high volume plastic packages
  - JEDEC Pub 95, registered outline drawings for micro packages
  - Dual Leadframe (SOT, SOIC, SSOP, TSSOP, PSOP, TSOP…)
- Hermetic packaging processes

Who Should Attend?
This overview course is intended for those unfamiliar with microelectronics packaging technology. People in sales, purchasing, program management, new engineers, managers, equipment/material suppliers, people new to this industry or anyone looking to get a broad industry overview and review of the industry drivers, history and future trends are welcome to attend.

Mr. Tom Green is the principle at TJ Green Associates LLC (www.tjgreenllc.com) a veteran owned small business focused on training and consulting for military, space and medical microelectronic devices. He teaches a variety of public courses around the globe and in plant at major corporations and consults for a variety of medical device companies. He has thirty two years of experience in microelectronics working at positions in industry, academia and government. Tom has demonstrated expertise in die attach, wirebond, visual inspection, hermetic seal and leak testing processes. He has gained valuable experience over the past ten years in packaging and testing of devices for use as Class III medical implants and is often called on as an expert witness for hermeticity related failures. Tom is an active IMAPS member and Society Fellow. He has a B.S. in Materials Engineering from Lehigh University and a Masters from the University of Utah.

PDC3: Introduction to Fan-Out Wafer Level Packaging
Course Leader: Beth Keser, Qualcomm Technologies, Inc.
Morning PDC: 8:00am – 12:00pm | $400 (Through 2/10/2016) - $450 (after 2/10/2016)

Course Description:
Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 8 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking. This course has been updated with over 10% new material compared to the first time it was offered last year at the IMAPS Device Packaging Conference.

Outline:
1. Current Challenges in Packaging;
2. Definitions and Advantages;
3. Applications;
4. Package Structures including Advanced FO technologies;
5. Process;
6. Material Challenges;
7. Equipment Challenges;
8. Design Rules;
9. Technology Roadmap;
10. Reliability;
11. Benchmarking

Who Should Attend?
Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Engineers and those in marketing and sales who supply equipment, materials, or services to the advanced packaging supply chain should also attend. Both newcomers and experienced practitioners are welcome.
Dr. Beth Keser has over 17 years’ experience in the semiconductor industry. Beth received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. in Materials Science and Engineering at the University of Illinois at Urbana-Champaign. Beth’s development of materials and packaging technologies for the semiconductor industry has resulted in 8 patents, 10 patents pending, and over 40 publications in this area. Currently, Beth is the Fan-Out Wafer Level Packaging Technology Manager at Qualcomm, San Diego.

Before joining Qualcomm in 2009, Beth Keser was instrumental in developing 2 packaging technologies during her career at Motorola and Freescale Semiconductor. Beth led the Wafer-Level Chip Scale packaging team at Motorola, which included directing the activities of process engineering, package characterization, package reliability, and mechanical modeling. In addition, Beth Keser was the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP). Beth led the team that developed this technology for 6 years. Beth developed several process and material solutions for this new technology. Beth also volunteered as WLP Track co-chair at IMAPS Device Packaging Conference from 2006-2009.

**PDC4: Electrical Modeling and Test Strategies for 3D Packages**

**Course Leader:** Bruce Kim, City University of New York  
*Course Description:*  
Today’s miniaturization and performance requirements result in the usage of high-density advanced packaging technologies, such as system-in-package (SIP), direct-chip-attach, chip-scale packaging (CSP), and ball-grid-arrays (BGA). Due to their physical access limitation, the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This course introduces comprehensive knowledge of electrical modeling and test solutions for 3D packages. We begin by a short tutorial on 3D packages including interposers and TSV. We then place particular emphasis on electrical modeling; test and debugging approaches for 3D packages for RF, bio, power and MEMS packages. Finally, we cover diagnosis and repair techniques for assembled packages.

**Course Outline:**
- What is 3D packaging?
- Introduction to existing 3D package techniques in
  - Analog/Digital RF device packages
  - Mixed-signal device packages
- New Research Electrical Test strategies
  - RF testing
  - Mixed-signal testing
  - MEMS/Nano testing
- 3D package modeling
- TSV inductor design
- 3D package testing
  - Interconnect modeling
  - Defect testing
  - Overview of existing techniques
  - Research substrate test strategies
- Repair/diagnosis techniques for modules
- Summary and Outlook

**Who Should Attend?**
This course is beneficial to all design and test engineers, scientists, technical managers, design and manufacturing personnel, and production staffs in automotive, consumer, communication, computer, and aerospace industries. Although the course reviews most recent advances in 3D packaging, the course does not assume prior knowledge of these issues and hence is of interest for both experts and newcomers in this area.

Dr. Bruce Kim is a professor of the Department of Electrical Engineering at City University of New York. He has about 300 publications in packaging and testing areas. He has instructed previous PDCs at IEEE EPTC and ECTC conferences. He is a Fellow of IMAPS and received the Outstanding Educator award in 2012. He has also been a student chapter advisor. His research interests are in 3D passive components and testing.

**PDC5: Performance-based Roadmaps for Advanced Packaging**

**Course Leader:** Dev Gupta, APSTL  
*Course Description:*  
There have been long delays in both the development and implementation of revolutionary new Adv. Packaging technologies such as 3-d stacking of dice using Thru Silicon Vias (TSVs), especially for high performance but cost driven systems e.g. Smart Phones, which per forecast should have happened by now. To avoid such misses it is necessary for developers of new Packaging technologies to understand SYSTEM performance issues as well. This is what we do in this half day course. We will examine in detail performance metrics e.g. signal integrity that limits the bandwidth of data transfer between a SoC and Memory in a Smart Phone, the power required to transfer this data and aspects of Package design that affect them. We will also review trends in future system & chip designs in terms of these parameters. Next we will explore the performance gaps in current packages that would require transition to other technologies including 2.5 and 3d die stacks. The packages examined are PoP, used extensively in Smart Phones and Tablets, as well as modules in Servers. Then we will examine various 2.5d and 3d technologies already implemented and / or under development and discuss the performance point at which these new and expensive technologies will become indispensable. Lastly we will examine some intermediate technologies that are more cost effective in improving performance and thus amenable to consumer systems.

**Who Should Attend?**
Planners, Managers and Engineers involved in developing and marketing Adv. Packaging solutions

Dr. Dev Gupta has been involved in pioneering and developing Adv. Packaging technologies that have now become industry standards. In the early ’90s at Motorola he led the team that developed electroplated solder bump flip chip technology and robotic bonding tools. Later he developed industry first micro pillar flip chip system including thermo-compression bonding and was put into mass production to build GaAs power amplifiers for mobile phones. At Intel Dr. Gupta managed the development of now standard organic substrates for flip chip microprocessors. At APSTL he has been working on low cost alternatives to TSV based die stacks. He is a frequent speaker and instructor at IEEE and IMAPS events.
PDC6: Introduction to Microelectronics Packaging (PART II)
Course Leader: Thomas Green, TJ Green Associates LLC
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/10/2016) - $450 (after 2/10/2016)

Course Description:
Advanced Micro Packaging and Emerging Technology

- QFP (Quad Flat Packs) - QFN (Quad flat No lead)
- BGA (Ball Grid Array) style packages
- Wafer-level packaging (WLP)
  - Wafer Level Chip Scale Packaging (WLCS)
  - Solder bumping processes
  - WLP (Fan In and Fan Out)
  - RDL (Redistribution Layers)
  - Stacked CSPs
- SIP (System in a Package)
- MCMs (Multi chip modules)
- POP (Package on package)
- PIP (Package in Package)
- Emerging technologies 2.5 to 3D
  - What is the difference? What are the trends?
- 3D Chip tacking
- TSVs (Through Silicon Via) for 3D stacking
- Interposer technology
  - Glass vs Silicon
- Integration of photonic devices
- Thermal design - How to get the heat out
  - Thermal resistance test methods and JESD51-2A
- Electrical design concerns from a packaging perspective
- Reliability of micro packages
  - Qualification testing of new package designs
  - Common failure modes
  - Plastic and hermetic type packages
- Industry Roadmaps

Who Should Attend?
This overview course is intended for those unfamiliar with microelectronics packaging technology. People in sales, purchasing, program management, new engineers, managers, equipment/material suppliers, people new to this industry or anyone looking to get a broad industry overview and review of the industry drivers, history and future trends are welcome to attend.

Mr. Tom Green is the principle at TJ Green Associates LLC (www.tjgreenllc.com) a veteran owned small business focused on training and consulting for military, space and medical microelectronic devices. He teaches a variety of public courses around the globe and in plant at major corporations and consults for a variety of medical device companies. He has thirty two years of experience in microelectronics working at positions in industry, academia and government. Tom has demonstrated expertise in die attach, wirebond, visual inspection, hermetic seal and leak testing processes. He has gained valuable experience over the past ten years in packaging and testing of devices for use as Class III medical implants and is often called on as an expert witness for hermeticity related failures. Tom is an active IMAPS member and Society Fellow. He has a B.S in Materials Engineering from Lehigh University and a Masters from the University of Utah.

PDC7: Emerging Challenges in Packaging
Course Leader: Raja Swaminathan, Intel Corporation
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/10/2016) - $450 (after 2/10/2016)

Course Description:
The course will begin with a broad description of electronic packaging types, functions, trends per industry to introduce the basic concepts of packaging. The first half of the course will focus on the key elements driving the definition of package architectures including form factor, z-height, cost, functional integration complexity, power delivery, high speed signaling and thermo-mechanical interactions with system, to name a few. The interactions between these elements towards enabling a successful package architecture for a given product will be reviewed with examples from different product segments (phones, tablets, PCs, servers etc.). The second half of the course will focus on the package, assembly, test and silicon integration and surface mount challenges towards enabling high volume manufacturing of the package architectures.

Who Should Attend?
The attendees are expected to have an in depth understanding of the fundamentals of packaging.

Dr. Raja Swaminathan is an IEEE senior member and is a package architect at Intel for next generation server, client and SOC products. His primary expertise is on delivering integrated HVM friendly package architectures with optimized electrical, mechanical, thermal solutions. He is an ITRS author and INEMI technical WG chair on packaging and design. He has also served on IEEE micro-electronics and magnets technical committees. He has 13 patents and 18 peer reviewed publications and holds a Ph.D in Materials Science and Engineering from Carnegie Mellon University.
PDC8: Polymers in Electronic Packaging
Course Leader: Jeff Gotro, InnoCentrix, LLC
Afternoon PDC: 1:00pm – 5:00pm | $400 (Through 2/10/2016) - $450 (after 2/10/2016)

Course Description:
The course will provide an overview of polymers and the important structure-property-process-performance relationships for electronic packaging. The main learning objectives will be: 1) learn how polymers are used in electronic packaging including die attach adhesives, underfills, mold compounds and substrate materials 2) gain insights on how polymers are used in 2.5D and 3D packaging, 3) learn the key polymer challenges and processes for 2.5D and 3D packaging, 4) learn how polymers testing procedures specific to electronic packaging are used 5) develop a foundation in rheology and rheology issues in electronic packaging. Participants are invited to bring problems for discussion.

Who Should Attend?
Packaging engineers involved in the development, production, and reliability testing of electronic packages would benefit. Those interested in gaining a basic understanding of the role of polymers and polymer-based materials used in electronic packaging will also find this PDC valuable.

Dr. Jeff Gotro has over thirty three years of experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. Jeff is a recognized authority in thermosetting polymers and has received invitations to speak at prestigious Gordon Research Conferences (Thermosetting Polymers and Composites). He has presented numerous invited lectures and short courses at technical meetings, has over 60 technical publications and 21 patents/patent applications. Jeff is a Fellow of IMAPS and was awarded the John A. Wagnon Technical Achievement Award in 2014 for his technical contributions in the area of polymers in electronic packaging. Jeff was an Adjunct Professor at Syracuse University in the Dept. of Chemical Engineering and Materials Science from 1986-1993. Jeff is a member of the American Chemical Society (ACS), the Institute for Management Consultants (IMC), the Forensic Expert Witness Association (FEWA), and IMAPS.

Welcome Reception: Monday, March 14, 5:00pm-7:00pm
(All Attendees Are Invited To Attend)

Thank you to the Device Packaging Welcome Reception Sponsors:

SPEAKER/PRESENTATION INFORMATION (DETAILS ON-LINE AT WWW.IMAPS.ORG/DEVICEPACKAGING)

Extended Abstract or Presentation Material due: February 10, 2016. Required for oral and poster presenters.
Send your extended abstract (2-4 pages) via email to bschieman@imaps.org, in PDF format only (no passwords). Your short papers will be included in the Conference MOBILE APP before the conference begins.

PowerPoint/Presentation file used during session: Speaker’s responsibility to bring to session on USB (recommended having back-up on personal laptop, or USB/memory stick). Laptops will be provided by IMAPS in the session room.

IMAPS will be producing a DOWNLOAD of presentations after the event. All speakers are asked to email a PDF copy of his/her presentation to Brian Schieman (bschieman@imaps.org) prior to the event, if possible; or the speaker’s PowerPoint slides that were saved on the session laptops will be used. If you have changes to your slides for the DOWNLOAD, you MUST submit the new file at the Registration Desk before the conference closing. Presentations not received before/during event will not be included in the DOWNLOAD.

Speakers must register for the conference at the reduced speaker rate. Early registration deadline is February 10, 2016. Visit www.imaps.org/devicepackaging for more information.
Device Packaging Exhibition and Technology Showcase
Exhibiting Companies

The exhibit hall is now **SOLD OUT, marking this the 11th consecutive year of a sellout – this year it sold earlier than ever before, and with more than 11 companies on a waitlist!** The following booths will be on display during Device Packaging 2016. Please visit the companies' websites listed below for more information. The floor plan of the exhibit hall is included on the following page as well. If you have questions about exhibiting with IMAPS, or about getting signed up for the 2017 Device Packaging Conference, contact Brian Schieman at bschieman@imaps.org.

<table>
<thead>
<tr>
<th>Company</th>
<th>Booth(s)</th>
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**Early Conference Registration & Hotel Reservations**

*Early Registration Rate and Hotel Block Pricing Ends: February 10, 2016*

Book your hotel reservation today! We have reserved a block of rooms at the host hotel to accommodate our attendees. The discounted room rates are only available until the hotel deadline listed above, or until the room block sells out (and they often sell out early - before the expire dates). Reservations received after the noted deadline or after the room block has been filled may be subject to significantly higher rates. IMAPS room blocks at most hotels historically sell out ahead of the discount deadline, so we encourage you to make your hotel reservations quickly for the best price and availability.

Online Registration & Hotel Reservations:

[www.imaps.org/devicepackaging](http://www.imaps.org/devicepackaging)
KEYNOTE – FAN-OUT: Localized High Density Interconnects with Intel’s EMIB

In recent years there has considerable interest in packages that enable high wiring density between die. This interest is motivated by the need for high inter-die bandwidth using wide and slow data busses as a means of achieving low power (i.e. low pJ/bit) interconnects. This talk provides an introduction to Intel’s high wiring density packaging technology i.e. EMIB (Embedded Multi-Die Interconnect Bridge) and compares it with other alternative technologies.

Ravi Mahajan, Senior Principal Engineer, Intel Corporation

Ravi Mahajan is a Senior Principal Engineer in the Path finding Group, part of Intel Corporation’s Assembly & Test Technology Development (ATTD) in Chandler, Arizona. He is responsible for setting technology directions for Packaging and Assembly processes for silicon at future nodes. He currently leads the Pathfinding effort for packaging @ the 7nm node. Ravi is also responsible for setting technical direction for Intel and consortia funded research in Assembly and Packaging. In this capacity he represents Intel in the Advisory Board of the Packaging Thrust in the Semiconductor Research Corporation. Ravi received a BS degree (University of Bombay, 1985), a MS degree (University of Houston, 1987) and a PhD degree (Lehigh University, 1992) in Mechanical Engineering. He specialized in Fracture Mechanics during his work towards his MS and PhD degrees. He has authored several technical papers in the areas of experimental and analytical stress analysis and thermal management. He holds several patents in the area of microelectronic packaging, most notably for the original concept of the Silicon bridge and for some of the very early cooling solutions for high power and high power density micro-electronics components. He has been Editor and one of the founding members for the Section on Micro-Electronics for the Society of Experimental Mechanics. He is also one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) an Intel internal journal that documents challenges and current progress in the area of Assembly & Packaging. Ravi is the Co-Editor for the Special Topics Section of IEEE T-CPMT journal. Ravi is a Fellow of two leading societies i.e. The American Society of Mechanical Engineers and IEEE.

KEYNOTE – FAN-OUT:

To Be Announced Soon

See www.imaps.org/devicepackaging

IMAPS 2016 Pasadena
Abstracts Due: March 31, 2016

Device Packaging Speakers can submit abstracts and papers for IMAPS 2016!
### Exhibition and Technology Showcase

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<th>Time</th>
<th>Interposers, 3D IC &amp; Packaging</th>
<th>Fan-Out, Wafer Level Packaging &amp; Flip Chip</th>
<th>SIP &amp; Engineered Micro Systems/Devices (including MEMS &amp; Sensors)</th>
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<tbody>
<tr>
<td>10:00 am – 10:30 am</td>
<td>Break in Exhibit Hall Sponsored by: Amkor Technology</td>
<td>TA1: 3D Devices and Architectures (incl. non-TSV alternatives to 3D, Design...) Chair: Rahul Agarwal, GlobalFoundries; Lars Boetscher, Fraunhofer Institute IZM</td>
<td>TA3: Fabrication and Packaging Technologies Chairs: Russell Shumway, Amkor Technology; Li-Anne Liew, NIST Boulder</td>
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<tr>
<td>10:30 am – 11:00 am</td>
<td>2016dpc051 - 2.5D / 3D IC Landscape: Market and Technology Trends Andrej Ivanovic, Yole Developpement (Thibault Buisson, Amandine Pizzagalli, Dave Towne, Rozalia Beica)</td>
<td>2016dpc074 - Embedded RDL Enabled by Excimer Laser Ablation Habib Hichti, SUSS MicroTec</td>
<td>2016dpc010 - Plasma Activated Bonding for an Enhanced Alignment Electrostatic Lens Elham Vakil Asadollahi, University of California, Irvine (Manuel Gamero-Castano)</td>
</tr>
<tr>
<td>11:00 am – 11:30 am</td>
<td>2016dpc082 - Testing in-package DRAMs and DFX features in 3D High-bandwidth Memory Chris Nelson, Intel Corporation</td>
<td>2016dpc026 - Enabling Next Generation M-WLCSP through Laser Dicing Jeroen van Borkulo, ASM Pacific Technology (Eric Tan, Eric Kuah)</td>
<td>2016dpc041 - Comparison of Hermetic Sealing Using SAC and SnPb Solder for a MEMS Pressure Sensor Maake Visser Taklo, SINTEF (Branson Belle, Joachim Seland Graff, Astrid-Sofie Vardoy, SINTEF; Elisabeth Ramsdal, GE Presents)</td>
</tr>
<tr>
<td>11:30 am – 12:00 pm</td>
<td>2016dpc036 - Cost Breakdown of 2.5D and 3D Packaging Chet Palesko, SavanSys Solutions LLC (Amy Palesko)</td>
<td>2016dpc077 - Extending WLCSP Packaging Technology Capabilities to Enable Miniaturized Sensor and MEMS Packaging Applications Ted Tessler, Huanian Technology - Flip Chip International</td>
<td>2016dpc013 - Advances in Aligned Wafer Bonding Enable by High Vacuum Processsing Eric Pabo, EV Group NA (Christoph Floetgen, Bernhard Rehban, Razek Nasser)</td>
</tr>
<tr>
<td>12:00 pm – 12:30 pm</td>
<td>2016dpc008 - Impact of Electrical and Thermal Stresses on TSV Radiofrequency Performance Anh Phuong Nguyen, IPDIA (Ulrike Lüders, CRISMAT; Frederic Voiron, IPDIA)</td>
<td>2016dpc078 - Characterization of Clean after Photore sist Removal from Wafers with Copper Pillars Kimberly Pollard, Dynaloy, a subsidiary of Eastman Chemical Company (Richie Peters, Michael Phenis, Don Plettscher)</td>
<td>2016dpc059 - 3D Printing of High Voltage Printed Wiring Boards Eric MacDonald, University of Texas at El Paso (Ryan Wicker, David Espalin, Andy Kwas, Peter Ruby, Craig Kief)</td>
</tr>
<tr>
<td>12:30 pm – 2:00 pm</td>
<td>Lunch in Exhibit Hall Sponsored by: ASE GROUP</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### Exhibition and Technology Showcase:

**Tuesday, March 15th**
10:00 am - 6:30 pm

**Wednesday, March 16th**
10:00 am - 4:00 pm

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A Special THANK YOU to our Device Packaging Premier Sponsors!

| ASE GROUP | Amkor Technology | NAMICS |

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A Special THANK YOU to our Corporate Sponsors!

<p>| SPTS | Mentor Graphics | EMD Performance Materials |</p>
<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
</tr>
</thead>
</table>
| 2:00 pm - 2:30 pm | Title Updated Online  
Mike Kelly, Amkor                                                                 |
| 2:30 pm - 3:30 pm | 2016dpc081 - Impact of Top Die Thickness on Cu Pillar Fatigue in Exposed Die 3D Packages  
Rahul Agarwal, GlobalFoundries (Sukesh Kannan, Shian Gao, Rick Reed, Yong Song, JS Paek) |
| 3:00 pm - 3:30 pm | 2016dpc023 - High-Speed Electroplating of 200um High Cu Bumps for Die Stacking Architectures  
Richard Hollman, TEL NEXX, Inc. |
| 4:00 pm - 4:30 pm | 2016dpc044 - Evaluation of High-Speed Copper Plating Products for RDL, Micropillar, and Fan-Out Applications  
Matthew Thorseth, Dow Chemical (Mark Scalisi, Inho Lee, Sang-Min Park, Yi-Hak Lee, Jonathan Prange, Masaaki Imanari, Mark Lefebvre, Jeff Calvert) |
| 4:30 pm - 5:00 pm | 2016dpc005 - Versatile Metrology Platform for FOWLP  
PnP Manufacturing Process Control  
Francy Abraham, Koh Young America Inc. |
| 5:00 pm - 5:30 pm | 2016dpc052 - Current Status and Future Prospects of Panel Level Packaging  
Santosh Kumar, Yole Development (Amandine Pizzagalli, Dave Towne, Thibault Buisson, Andrej Ivanjkoic, Rozalia Beica) |
| 5:00 pm - 6:30 pm | Reception in Exhibit Hall Sponsored by:  
Mentor Graphics  
EMD Performance Materials |

**Afternoon Technical Sessions**

<table>
<thead>
<tr>
<th>Interposers, 3D IC &amp; Packaging</th>
<th>Fan-Out, Wafer Level Packaging &amp; Flip Chip</th>
<th>SiP &amp; Engineered Micro Systems/Devices (including MEMS &amp; Sensors)</th>
</tr>
</thead>
</table>
| TP1: 3D Device Fabrication Processes, Materials and Yield (Part 1)  
Chairs: Jeff Calvert, Dow Electronic Materials; Diane Scheele, Dynaloy-Eastman | TP2: Fan-Out Wafer Level Packaging  
Chairs: John Hunt, ASE US; Chris Scanlan, Deca Technologies | TP3: MEMS Devices and Sensors  
Chairs: Keaton Rhea, Auburn University; Eric MacDonald, University of Texas El Paso |

**Break in Exhibit Hall Sponsored by:**

**Amkor Technology**

- **4.00 pm - 4.30 pm**  
2016dpc016 - Thin WLFO and based WLSIP Enabling WL3D, Realized Using Temporary Reconstituted Panel Bonding Technology  
Steffen Kroesbier, NANIUM S.A. (Jose Campos, Andre Cardoso, Mariana Pires, Eon O’Toole, Raquel Pinto, NANIUM S.A.; Emile Jolivet, Thomas Uhrmann, Elizabeth Brandl, Juergen Burggraf, Harald Wiesbauer, Julian Bravin, Markus Wimplinger, Paul Lindner, EV Group) |

- **4.30 pm - 5.00 pm**  
2016dpc067 - Fan-Out Wafer Level Packaging: Market and Technology Trends  
Andrej Ivanjkoic, Yole Development (Jerome Azemar, Thibault Buisson, Rozalia Beica) |

- **5.00 pm - 5.30 pm**  
2016dpc083 - Ultra Fine Pitch RDL Development in Multi-layer eWLB Packages  
Bennie Adams, STATS ChipPAC (WK Choi, DJ Na, KO Aung, Andy Yong, SW Yoon, STATS ChipPAC, Jaesik Lee, Urmia Ray, Riko Radjopic, Qualcomm) |

- **5.00 pm - 6.30 pm**  
2016dpc050 - Terahertz Diode Arrays and Differential Probes based on Heterogeneous Integration and Silicon Micromachining  
Robert Weikle, University of Virginia (C. Zhang, S. Hawasli, S. Nadi, L. Xie, N. Scott Barker, A.W. Lichtenberger) |

**GBC Speaker Dinner | 8:00 pm**

*(By Invitation Only)*

**Thank you to the GBC Speaker Dinner Sponsors:**

- **ASE Group**
- **Amkor Technology**
- **NAMICS**
EVENING PANEL DISCUSSION ON SiP

Panel Discussion Refreshments & Food sponsored by:

SiP: New Drivers and the Supply Chain

System-in-Package (SiP) is a subsystem functional block integrating multiple ICs and often passives in a single package. SiPs are increasingly being adopted in a variety of applications ranging from wearables and mobile devices to high performance computing and automotive electronics. This panel explores the drivers for SiP with perspectives from representatives actively involved in the industry infrastructure. This panel brings together a panel representing the foundry, OSAT, EMS, foundry, and customer in the SiP supply chain. Challenges in the expansion of SiP will be discussed.

Moderator: E. Jan Vardaman, President, TechSearch International

Panelists:
- Robert Lanzone, Sr. VP/AVL&PD, Amkor Technology
- Joan Vrtis, CTO, Multek Technologies Innovation Labs
- Rich Rice, Sr. VP of Sales/Eng North America, Business Development, ASE

ADDITIONAL PANELISTS ADDED SOON

Download the Device Packaging 2016 MOBILE APP

The DPC 2016 mobile app features:
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- Speaker details and abstracts
- Session description
- Searchable and sortable attendee list
- Sortable and searchable exhibitor list
- Info, Links, and News
- Conference updates and changes
- Twitter feed

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2. Log in with your registration email and the password device16.
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Same great features with no download required at https://imaps.gatherdigital.com!
WEDNESDAY, MARCH 16, 2016  
GBC Keynote & Plenary Session

7:00 am – 8:00 pm  
Registration

7:00 am – 8:00 am  
Continental Breakfast Sponsored by:

8:00 am – 8:15 am  
Welcome to the Global Business Council (GBC) Keynote & Plenary Session on System Integration and Package Assembly Supply Chain Implications

OPENING COMMENTS:
GBC Chairs: Lee Smith, (UTAC) United Test & Assembly Center; Rich Rich, ASE Group

8:15 am – 9:00 am  
GBC KEYNOTE:  
Are IC Industry Cycles Dead or Just Sleeping?  
Although a high level of uncertainty still looms over the global economy, sales of smartphones continue to reach new highs and the Internet of Things looms on the horizon. IC Insights will present its forecast for the IC market and unit volume shipments in the context of the IC industry cycle model. In order to make sense out of the current turmoil, a top-down analysis of the IC market will be given and include trends in worldwide GDP growth, electronic system sales, and semiconductor industry capital spending and capacity.

Bill McClean, President  
IC INSIGHTS, INC.

Mr. McClean began his market research career in the integrated circuit industry in 1980 and founded IC Insights in 1997. During his 34 years of tracking the IC industry, Mr. McClean has specialized in market and technology trend forecasting and was responsible for developing the IC industry cycle model. At IC Insights, he serves as managing editor of the company’s market research studies and reports. In addition, he instructs for IC Insights’ seminars and has been a guest speaker at many important annual conferences held worldwide (e.g., SEMI’s ISS and Electronic Materials Conferences, The China Electronics Conference, and The European Microelectronics Summit). Mr. McClean received his Bachelor of Science degree in Marketing and an Associate degree in Aviation from the University of Illinois.

9:00 am – 9:30 am  
Hardware Opportunities for a Connected World  
E. Jan Vardaman, President  
TECHSEARCH INTERNATIONAL

9:35 am – 10:00 am  
SiP Trends in Handsets and Wireless Apps  
Rozalia Beica, Chief Technology Officer  
YOLE DEVELOPPEMENT

10:00 am – 10:45 am  
Exhibition and Technology Showcase

10:45 am – 11:15 am  
IC Industry Consolidation and Outlook with China Targeting $$ to Attain a Significant Share of IC Manufacturing  
Jim Walker, Research VP Semiconductor Manufacturing  
GARTNER TECHNOLOGY AND SERVICE PROVIDER RESEARCH

11:15 am – 12:15 pm  
Rao Tummala, Director, 3D Microsystems Packaging Research Center, GEORGIA INSTITUTE OF TECHNOLOGY

11:45 am – 12:00 pm  
GBC Plenary Session Closing Remarks
EMD Performance Materials

Performance Materials comprises the entire specialty chemicals business of Merck KGaA, Darmstadt, Germany. The portfolio includes high-tech performance chemicals for applications in fields such as:

- Displays
- Integrated Circuits
- Lighting Applications
- Solar & Energy
- Cosmetics, Food & Pharmaceuticals
- Coatings
- Semiconductor Packaging
- Printing & Plastics

We have established ourselves as the global market and technology leader in liquid crystal mixtures. Our company has the broadest product offering in the industry meeting individual customer needs and offering solutions for all display sizes, from smartphones and tablet computers to large-size television screens. Our portfolio also comprises materials that are used in integrated circuits. Furthermore, we develop and market a comprehensive product portfolio of decorative effect pigments and functional materials. The effect pigments are primarily used in automotive and industrial coatings, plastics, printing applications, and cosmetics in order to give products a unique shine.

We are extending our leading position in innovation Customers from the sectors consumer electronics, lighting, printing technology, plastics applications and cosmetics make use of materials and solutions from EMD Performance Materials. Thanks to comprehensive investments in research & development, we are constantly extending our leading position as an innovator and reliable partner.

A focus on sustainability Particularly in light of climate change, high energy prices and current events related to nuclear energy, we are focusing on sustainable materials. Our company is active in the growing markets of energy-saving LEDs for lighting, OLEDs for displays and lighting and materials for clean energies. Here the company is working on innovative photovoltaic materials for technologies that enable solar energy to be used efficiently.
### Afternoon Technical Sessions

#### Interposers, 3D IC & Packaging

<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
<th>Speaker Details</th>
</tr>
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<tbody>
<tr>
<td>1:30 pm - 2:00 pm</td>
<td>2016dpc076 - Packaging and Assembly Challenges for 2.5D/3D Devices</td>
<td>Gerald Beyer, IMEC (Kenneth Reibis, Anita Podpod, Francisco Calacito, Teng Wang, Andy Miller, Eric Beyne)</td>
</tr>
<tr>
<td>2:00 pm - 2:30 pm</td>
<td>2016dpc045 - Non-Conductive Film (NCF) Underfill: Materials, Performance, and Evolution to Next Generation Devices</td>
<td>Paul Morganelli, Dow Electronic Materials (Edgaro Anzuers, Robert Barr, Jeffrey Calvert, Amin Dhoble, David Fleming, Jong-Uk Kim, Herong Lei, Dow Electronic Materials; Juergen Grafe, Julian Haberland, Fraunhofer IZM)</td>
</tr>
<tr>
<td>3:00 pm - 4:00 pm</td>
<td>Break in Exhibit Hall Sponsored by: Amkor Technology®</td>
<td></td>
</tr>
<tr>
<td>4:00 pm - 4:30 pm</td>
<td>2016dpc034 - Critical Process Parameters And Failure Analysis For Temporary Bonded Wafer Stacks</td>
<td>Elisabeth Brandl, EV Group (Karine Abadie, Markus Wimpflinger, Juergen Burggraf, Thomas Uhmann, Julian Bravin, EV Group; Frank Foumat, Pierre Montreat, Univ. Grenoble/CEA)</td>
</tr>
<tr>
<td>4:30 pm - 5:00 pm</td>
<td>2016dpc028 - TCB Process Options to Achieve the Lowest Cost</td>
<td>Tom Strothmann, Kulicke &amp; Soffa Industries, Inc.</td>
</tr>
<tr>
<td>5:00 pm - 5:30 pm</td>
<td>2016dpc075 - Photolithography Alignment Mark Transfer System for Low Cost, Advanced Packaging and Bonded Wafer Applications</td>
<td>Steve Gardner, Rudolph Technologies (Casey Donaher, Keith Best)</td>
</tr>
</tbody>
</table>

#### Fan-Out, Wafer Level Packaging & Flip Chip

<table>
<thead>
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<tbody>
<tr>
<td>1:30 pm - 2:00 pm</td>
<td>2016dpc021 - Advancements in Flip Chip Assembly Equipment and Processes</td>
<td>Bob Chylak, Kulicke and Soffa (Horst Clauberg, Daniel Buergi)</td>
</tr>
<tr>
<td>2:00 pm - 2:30 pm</td>
<td>2016dpc025 - V-DOE Full Cut Dicing of Thin SiIC Wafers</td>
<td>Jeroen van Borkulo, ASM Pacific Technology (Paul Verbunt, Eric Tan)</td>
</tr>
<tr>
<td>2:30 pm - 3:00 pm</td>
<td>2016dpc068 - Emerging Flux Challenges for BGA Packages</td>
<td>Maria Durham, Indium Corporation (Jason Chou-Area)</td>
</tr>
<tr>
<td>3:00 pm - 4:00 pm</td>
<td>2016dpc031 - Washable Coatings for Packaging Practices</td>
<td>John Moore, Daetec LLC (Alex Brewer)</td>
</tr>
<tr>
<td>4:00 pm - 4:30 pm</td>
<td>2016dpc032 - Precise, High Throughput Dispensing of Thermal Interface Material in BGA Packaging Applications</td>
<td>Hanzhua Liang, Nordson Asymtek (Linh Hanzhuang Liang, Nordson Asymtek (Linh Packard))</td>
</tr>
<tr>
<td>4:30 pm - 5:00 pm</td>
<td>2016dpc039 - A Matched Filter Developed for Chaotic Wavesforms</td>
<td>Frank Werner, Auburn University (Benjamin Rhea, Auburn University; Frank Werner, Remington Harrison, Robert Dean)</td>
</tr>
<tr>
<td>5:00 pm - 5:30 pm</td>
<td>2016dpc066 - Advanced Substrate Landscape: Market and Technology Trends for Silicon and Organic Solutions</td>
<td>Andrej Ivanovsk, Yole Development (Thibault Buissen, Amanda Pizzagalli, Santosh Kumar, Dave Towne, Rozalia Beica)</td>
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#### Engineered Micro Systems/Devices (Including MEMS & Sensors)

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</thead>
<tbody>
<tr>
<td>1:30 pm - 2:00 pm</td>
<td>2016dpc057 - A Survey of Nonlinear Phenomena and Chaos in Microsystems and Packaging</td>
<td>Aubrey Beal, Charles M. Bowden Laboratory, U.S. Army-ARDEC (Robert Dean)</td>
</tr>
<tr>
<td>2:00 pm - 2:30 pm</td>
<td>2016dpc063 - Nonlinear Dynamics Induced Anomalous Hall Effect in Topological Insulators</td>
<td>Guanglei Wang, Arizona State University (Hongya Xu, Ying-Cheng Lai)</td>
</tr>
<tr>
<td>2:30 pm - 3:00 pm</td>
<td>2016dpc038 - A Novel Third Order Analog Chaotic Oscillator</td>
<td>Benjamin Rhea, Auburn University (Frank Werner, Remington Harrison, Robert Dean)</td>
</tr>
<tr>
<td>3:00 pm - 4:00 pm</td>
<td>2016dpc072 - Nonlinear Dynamics and Chaos in Micro/Nano-Scale Systems and Applications</td>
<td>Ying-Cheng Lai, Arizona State University (Hongya Xu, Ying-Cheng Lai)</td>
</tr>
<tr>
<td>4:00 pm - 4:30 pm</td>
<td>2016dpc070 - Nonlinear Dynamics and Chaos in Micro/Nano-Scale Systems and Applications</td>
<td>Ying-Cheng Lai, Arizona State University (Hongya Xu, Ying-Cheng Lai)</td>
</tr>
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#### SIP New Sessions for 2016!

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<td>Andrej Ivanovsk, Yole Development (Thibault Buissen, Amanda Pizzagalli, Santosh Kumar, Dave Towne, Rozalia Beica)</td>
</tr>
</tbody>
</table>
Interactive Poster Session & “Happy Hour”

5:30 pm - 6:30 pm
(Poster setup: 4:00 pm - 5:00 pm)
Outside on the Patio/Grass – Weather Permitting

2016dpc024 – 3D
Improvements in Decision Making Criteria for Thermal Warpage
Neil Hubble, Akrometrix

2016dpc037 – 3D
Wafer-Level Packaging For Ultra-Thin Glasses Using Hermetic Room Temperature Welding Technology
Antti Peltonen, Primoceler Oy (Heidi Lundén, Antti Määttänen)

2016dpc055 – 3D
Application of Mathematical Modeling to Thermo-Compression Flip Chip Bonding of Copper Micro Pillar Bumps for 3D Die Stacking
Dev Gupta, APSTL, LLC

2016dpc069 – 3D
Design of TSV-based Inductors for Internet of Things
Bruce Kim, City University of New York (Saikat Mondal)

2016dpc073 – 3D
Cost Analysis of a Wet Etch TSV Reveal Process
Laura Mauer, Veeco Precision Surface Processing (John Tadder; Amy Palesko Lujan, SavanSys Solutions LLC)

2016dpc006 – FC/FO/WLP
Impact of Cleaning Technologies on Lead Frame Packages: The Difference in Wire Bond Yields
Guan Tatt Yeah, ZESTRON
(Umut Tosun, Ravi Parthasarathy, ZESTRON Americas)

2016dpc017 – MEMS/Sensors
Portable System Design for Post-tensioned Prestressed Ducts Based on Coplanar Capacitive Sensor
Nan Li, Beijing University of Technology (Mingchen Cao, Kai Liu)

2016dpc030 – SiP
The Effects of Surface Finish on the Microstructure of Sintered Paste Joints
Catherine Shearer, Ormet Circuits, Inc.

2016dpc032 – 3D
Reliability of Copper Pillar Devices Assembled using One Step Chip Attach Materials and (OSCA-R) Conventional Mass Reflow Processing
Daniel Duffy, Kester Inc. (Hemal Bhavsar, Lin Xin, Jean Liu, Bruno Tolla)

2016dpc038
Numerical Simulation of Copper Migration in Single Crystal CdTe
Da Guo, Arizona State University (Dragica Vasileska)

2016dpc008
Numerical Simulation of Copper Migration in Single Crystal CdTe
Da Guo, Arizona State University (Dragica Vasileska)

2016dpc071
TCAD Modeling of InGaN-Based High Temperature Photovoltaic Solar Cell
Yi Fang, Arizona State University (Dragica Vasileska, Stephen Goodnick)

2016dpc079
Next Level of Enhanced Isotropic Etchants
R. Haider, Atotech Deutschland GmbH (P. Brooks, F. Michalik, N. Luetzow, G. Schmidt, T. Huelsmann, M. Klopstch)

2016dpc081
New Uses of Excimer Laser Technology in the Packaging Industry
Dirk Mueller, Coherent Inc. (Rainer Patzelz)

2016dpc007
A Study on Warpage Behavior of EMC in Post-mold Cure Stage using Moldex3D
Hsu Chih-Chung, CoreTech System (Moldex3D) Co., Ltd. (Srikar Vallury, Kai Lin, Anthony Yang)

Hotel Cut-off: FEBRUARY 10, 2016

WeKoPa Resort | Fountain Hills, AZ 85264
IMAPS Discounted Single/Double Room Rate:
$169/night + Taxes and Fees

Online Reservations at www.imaps.org/devicepackaging

Phone Reservations: (480) 789-5300

Mention IMAPS or IMAPS Device Packaging when booking by phone

Book your hotel reservation today! We have reserved a block of rooms at the host hotel to accommodate our attendees. The discounted room rates are only available until the hotel deadline listed above, or until the room block sells out (and they often sell out early - before the expire dates). Reservations received after the noted deadline or after the room block has been filled may be subject to significantly higher rates. IMAPS room blocks at most hotels historically sell out ahead of the discount deadline, so we encourage you to make your hotel reservations quickly for the best price and availability.
<table>
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<td>7:00 am – 11:00 am</td>
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<td>Continental Breakfast Sponsored by: NAMICS</td>
</tr>
<tr>
<td>8:00 am – 8:45 am</td>
<td>Keynote Sessions Sponsored by: SPTS</td>
</tr>
<tr>
<td>8:45 am – 9:30 am</td>
<td>Break in Foyer Sponsored by: Amkor Technology</td>
</tr>
<tr>
<td>9:30 am – 9:45 am</td>
<td>ISTS: 3D: Keynote To Be Announced Soon See <a href="http://www.imaps.org/devicepackaging">www.imaps.org/devicepackaging</a></td>
</tr>
<tr>
<td>9:45 am – 10:45 am</td>
<td>2016dpc047 - Innovated Process Integration for Panel Size Glass Substrate Manufacturing for SIP Application Yu-Hua Chen, Unimicron Technology Corp. (Yu-Chung Hsieh, Wei-Di Lin, Chun-Hsien Chien, Dyi-Chung Hu)</td>
</tr>
<tr>
<td>11:15 am – 11:45 am</td>
<td>2015dpc032 - Embedded Die Packages and Modules for Power Electronics Applications Lars Boettcher, Fraunhofer IZM (S. Karszewski, D. Manessis, A. Obstmann)</td>
</tr>
</tbody>
</table>

**Interposers, 3D IC & Packaging**

- **THA1:** 2.5D/Advanced Packaging (Others: RF, Integrated Passives, Medical,...)
  - Chairs: Franck Murray, IPDIA; Eric Pabo, EV Group

- **THA2:** Fan-Out, Wafer Level Packaging & Flip Chip
  - 2016dpc014 - Low profile Flip-Type or Embedded Silicon Capacitors for decoupling
    - Catherine Bune, IPDIA (Franck Murray)

- **THA3:** SIP & Engineered Micro Systems/Devices (including MEMS & Sensors)
  - 2016dpc020 - How Mitigation Techniques Affect Reliability Results for BGAs
    - Greg Caswell, DfR Solutions (Melissa Keener)

- **THA4:** New Sessions for 2016!
  - 2016dpc049 - Design of High Density SIP for Complex Computing System in Micro SD Format
    - Chris Barret, Insight SIP
Thursday, March 17, 2016
1:00pm Shotgun Start – “Best Ball” Scramble

SunRidge Canyon Golf Club
13100 N Sunridge Dr | Fountain Hills, AZ 85268

The IMAPS Microelectronics Foundation Spring Golf invitational will be held at SunRidge Canyon’s 6,823-yard, par-71, Keith Foster-designed golf course unfolds around the rugged ridges and shady canyons unique to the desert mountains that divide Fountain Hills from Scottsdale, Arizona. This Scottsdale golf course gradually descends on the way out before doubling back to climb up the slope on the way in. This subtle elevation change lies at the heart of the dramatic golf experience at SunRidge Canyon.

Cost: $150/golfer
The cost includes: Transportation to and from the course, greens/cart fees, shotgun start, and an awards buffet reception following your round.

A shuttle will pick up golfers at the Radisson Fort McDowell at 12:00pm. Golfers will tee off shortly after arriving at the course – 1:00pm shotgun start. Golfers are welcome to drive themselves to arrive earlier. An awards presentation and reception will be held immediately following golf.

Special Awards and Activities tentatively planned:
- Closest to the Pin;
- Longest Drive;
- Dixon Golf’s Driving Accuracy & Hole-in-One (New) Competitions

Sponsorship Opportunities:

Eagle Sponsor - $3,000
- Company logo/name displayed as Awards Reception Sponsor.
- Entrance of two four-somes.
- Includes three hole sponsorships with signage.
- Company logo/name on all event promotional signs, materials and website.
- Company may provide take-away products to be handed to all golfers. Golf-related items usually most appropriate (e.g., golf towels, balls, tees, etc.). At expense of sponsor.

Birdie Sponsor - $1,500
- Company logo/name displayed as Lunch Sponsor - in/on boxed lunches.
- Entrance of one four-some.
- Includes one hole sponsorship with signage.
- Company logo/name on all event promotional signs, materials and website.

Hole Sponsor - $475 (includes 1 golfer) or $800 (includes 4-some)
- Sponsorship of one hole with signage.
- Entrance of one/four golfer(s).
- Company logo/name on promotional materials and website.

Questions or request teams/partners:
David Virissimo, Foundation Golf Chair - David.Virissimo@ametek.com
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<tr>
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<td>Premier Corporate/Academic institutions</td>
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<td>Associate Corporate</td>
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<td>Affiliate (International chapters/unemployed members)</td>
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<td>Student</td>
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Additional Sponsorship still available - contact Brian Schieman at bschieman@imaps.org if you are interested in sponsoring DPC 2016, and gaining great exposure to the attendees.
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