

IMAPS International Conference and Exhibition on

Device Packaging

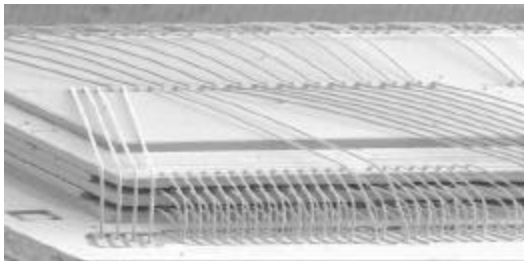
March 13 - 16, 2005

Hilton Scottsdale Resort & Villas
Scottsdale, Arizona - USA

Co-located with the Global Business Council (GBC) - Winter Conference 2005
March 16 - 17, 2005



www.imaps.org/gbc



Courtesy of STATSchipPAC Inc.

General Chair:

R. Wayne Johnson, Auburn University
johnson@eng.auburn.edu

Technical Co-Chairs:

Andrew Strandjord, IC Interconnect
astrandjord@icinterconnect.com

Theodore Tessier, ST Assembly Test
Services Inc.

ted.tessier@statschippac.com

Sponsored by:



International Microelectronics And
Packaging Society (IMAPS)

*"Everything in electronics between the chip
and the system"*

DEVICE PACKAGING PROGRAM OVERVIEW

Professional Development Courses - 1/2 Day

Sunday, March 13: 1 pm - 5 pm

Thermal Management Materials - PDC1

Instructor: Carl Zweben, Advanced Thermal Management Materials
Consultant

Flip Chip Assembly - PDC2

Instructor: R. Wayne Johnson, Auburn University

Hermeticity Testing and Issues with RGA - PDC3

Instructor: Thomas J Green, Microelectronics Packaging Consultant

Technical Sessions

Monday, March 14 - Wednesday, March 16

Session 1: Plenary

Session 2: Design/Modeling

Session 3: Wafer Bumping

Session 4: MEMS

Session 5: Materials

Session 6: SiP/3D Packaging

Session 7: Optoelectronics

Session 8: Process Technology

Session 9: Flip Chip Packaging

Exhibition

Monday, March 14 - Tuesday, March 15

10 am - 7 pm

9 am - 5 pm

Early Bird Registration and Hotel Deadline: February 1, 2005

*M*essage from the Chairs:

The members of the conference organizing committee are pleased to invite you to the IMAPS 1st International Device Packaging Conference in Scottsdale, Arizona. This event is intended to address emerging packaging requirements in key device applications including flip chip, 3 D packaging, System in Package (SiP), MEMS and optoelectronics.

The 1st International Device Packaging Conference will provide a comprehensive technical program addressing the challenges of applications, and the latest developments in packaging for emerging devices, circuits, MEMS, sensors as well as materials and processes. This meeting has also been structured so as to provide opportunities for networking and interaction with speakers, session chairs and other attendees; many of which are industry leading authorities in their respective areas of packaging. Tabletop exhibits will complement the technical program by providing you an opportunity to view the latest packaging related products and services.

For those wishing to broaden their knowledge of device packaging, a selection of half day short courses will be offered on the Sunday afternoon preceding the conference.

In addition to an outstanding technical program, you could also attend the Global Business Council (GBC) Winter Conference 2005, March 16 & 17, view the program inside or visit www.imaps.org/gbc for more information.

Please join us in sunny Scottsdale, where you can enjoy fabulous spring weather and the numerous natural attractions that Arizona offers amidst the excitement of Major League Baseball's Spring Training - Cactus League.

General Chair

R. Wayne Johnson, Auburn University

Technical Program Co-Chairs

Ted. G. Tessier, STATSChipPAC Inc.

Andrew Strandjord, IC Interconnect

Professional Development Courses - Sunday, March 13

Registration: Noon

Professional Development Courses (1/2 Day): 1 pm – 5 pm

Thermal Management Materials - PDC1

Instructor: Carl Zweben, Advanced
Thermal Management Materials
Consultant

COURSE DESCRIPTION:

In response to increasingly critical cooling problems, there have been revolutionary advances in thermal management materials in the last few years. There are now over a dozen low-CTE (coefficient of thermal expansion) materials with thermal conductivities between that of copper (400 W/m-K) and 1700 W/m-K, and almost a score with thermal conductivities at least 50% greater than that of aluminum (200 W/m-K). Some of these materials are low cost. Others have the potential to be low cost in high-volume production. Most have low densities. A number are being used in production applications, marking historic packaging milestones. These materials have broad applicability in microelectronic, optoelectronic and MEMS packaging. These new materials are revolutionary because traditional low-CTE thermal management materials, like copper/tungsten and copper/molybdenum, have thermal conductivities that are no better than that of aluminum (200 W/m-K). Advanced materials also offer a wide range of electrical properties that can be used to minimize electromagnetic emissions or provide EMI shielding. Payoffs include: improved thermal performance; reduced thermal stresses and warpage improved alignment; simplified thermal design; possible elimination of thermal interface materials, liquid cooling and heat pipes; weight savings up to 85%; size reductions up to 65%; increased reliability; increased manufacturing yield; and potential device and system cost reductions. This course covers traditional packaging materials and the large and increasing number of advanced materials, including: monolithic materials, metal matrix composites, polymer matrix composites, ceramic matrix composites, and carbon matrix composites. Topics include properties, manufacturing processes, development status, applications, and future directions.

THE INSTRUCTOR:

Dr. Zweben, an independent consultant, has directed development and application of advanced packaging materials for over 30 years. For many years, he was Advanced Technology Manager and Division Fellow at GE Astro Space, later acquired by Lockheed Martin, where he directed the Composites Center of Excellence. Other affiliations have included DuPont, Jet Propulsion Laboratory and the Georgia Institute of Technology NSF Packaging Research Center. Dr. Zweben was the first, and one of only two winners of both the GE One-in-a-Thousand and Engineer-of-the-Year awards. He is a Fellow of ASME, ASM and SAMPE, an Associate Fellow of AIAA, and has been a Distinguished Lecturer for AIAA and ASME. He has published and lectured widely on advanced thermal management and packaging materials.

Flip Chip Assembly - PDC2

Instructor: R. Wayne Johnson, Auburn
University

COURSE DESCRIPTION:

Flip chip use is growing in both flip chip-in-package and flip chip-on-laminate applications. This course will provide insight into the design and assembly of electronics using flip chip devices. The practical issues of implementing flip chip technology from wafer bumping to reliability characterization are covered. This course will begin with an examination of bumping options and corresponding design rules. Redistribution will also be discussed. Substrate requirements for flip chip will then be presented including a discussion of high density interconnect options and substrate design. Assembly of flip chip devices adds materials and processes to the standard SMT assembly process and the integration of these into the SMT process flow is examined. Materials and processes to be discussed include lead free alloys, fluxes, underfills (capillary flow, fluxing no-flow, and wafer applied), substrate dehydration, flux and underfill application, underfill curing, inspection, and underfill characterization techniques. The presentation will conclude with a discussion of flip chip assembly reliability testing, test vehicle design and failure analysis.

THE INSTRUCTOR:

Dr. Johnson is an Alumni Professor of Electrical Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). At Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and reliability for electronics assembly. He has worked in MCM design, MCM-L, -C and -D substrate technology as well as advanced SMT, wire bond and flip chip assembly techniques. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written two book chapters in the areas of silicon MCM technology and MCM assembly. He received the 1997 Auburn Alumni Engineering Council Senior Faculty Research Award for his work in electronics packaging and assembly. Dr. Johnson was the 1991 President of the Society. He received the 1993 John A. Wagnon, Jr. Technical Achievement Award from ISHM, was named a Fellow of the Society in 1994 and received the Daniel C. Hughes Memorial Award in 1997. He is also a member of IEEE, SMTA, and IPC. Dr. Johnson received the B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering. He has worked in the microelectronics industry for DuPont, Eaton, and Amperex.

Hermeticity Testing and Issues with RGA - PDC3

Instructor: Thomas J Green,
Microelectronics Packaging Consultant

COURSE DESCRIPTION:

Hermeticity of electronics packages and hermeticity test techniques continue to be of critical importance to the microelectronics packaging community. Specifically, in the area of MEMS/MOEMS packaging, OLEDs, wafer scale packaging, optoelectronic devices and packaging for Military and Space. In addition, there are a host of medical implants, bio medical devices and emerging nanotechnology applications that all require hermetic packages and valid techniques to measure the leak rate. This course begins with an overview of hermetic sealing processes e.g. seam welding (also known as brazing), laser welding; solder sealing and techniques/methods to seal components at the wafer level.

The class will then examine the accepted leak test techniques as prescribed in Mil Standard 883 Test Method 1014. This misunderstood test method is often a source of frustration. The basic science behind helium fine leak testing (both the fixed and flexible methods) will be presented to the class along with the advantages and potential pitfalls of helium fine leak testing. Difficulties and limitations in fine leak testing of small volume packages is a major industry concern, especially among the Space community. Issues with bomb times and pressures, measured leak rate vs air leak rates, "one way leakers", virtual leakers will be addressed, along with gross leak testing; bubble, weight gain and other techniques such as dye penetrant. In each case the focus will be on practical issues facing the industry.

THE INSTRUCTOR:

Mr. Green is a consultant and adjunct professor at the National Training Center for Microelectronics. At NTC he designs curriculum and teaches industry short courses relating to advanced microelectronics manufacturing processes. He has over twenty years experience in the microelectronics industry at Lockheed Martin Astro Space and USAF Rome Laboratories. At Lockheed he was a Staff engineer responsible for the materials and manufacturing processes used in building custom high reliability space qualified microcircuits (Hybrids, MCMs and RF modules) for military and commercial communication satellites. Tom has demonstrated expertise in seam sealing and leak testing processes. He has conducted experiments and presented technical papers at NIST and IMAPS on leak testing techniques and optimization of seam welding processes through statistical DOE methods. At Rome Labs he worked as a senior reliability engineer and analyzed component failures from AF avionic equipment along with providing technical support for a variety of Mil specs and standards (e.g. MIL-PRF-38534 and MIL-STD-883). Tom is an active member of the IMAPS and is currently the chairman of the Optoelectronics National Technical Committee. He has a B.S. in Materials Engineering for Lehigh University and a Masters from the University of Utah.

Sunday, March 13

Registration: Noon - 5:30 pm

Opening Reception: 5 pm - 6 pm

Monday, March 14

Registration: 7:30 am – 7 pm

Continental Breakfast: 7:30 am

Exhibit Hours: 10 am – 7 pm

SESSION 1: PLENARY

Chairs: Ted Tessier, ST Assembly Test Services Inc.; Andrew Strandjord, IC Interconnect
8 am – 12:30 pm

Developments and Trends in 3D Packaging
Flynn Carson, ChipPAC, Incorporated

Wafer Bumping
Peter Elenius, E&G Technology Partners LLC

Break in Exhibit Hall: 10 am – 10:30 am

Wafer Level MEMS Packaging Strategies
Daniel Baldwin, Engent, Inc.

WLCSP Technology Direction
Michael Toepper, Fraunhofer IZM

Lunch in Exhibit Hall: 12:30 pm – 1:30 pm

Device Packaging Exhibition

“An opportunity to talk to industry leaders”

Exhibit Hours

Monday - March 14 10 am - 7 pm
Lunch, Refreshment Breaks and a Reception will be held in the Exhibit Hall.

Tuesday - March 15 9 am - 5 pm
Lunch, Refreshment Breaks and a Reception will be held in the Exhibit Hall.

Exhibit Registration Fees

	On/Before 2/1/05	After 2/1/05
IMAPS Corporate Member	\$1,100	\$1,300
Non-Corporate Member	\$1,700	\$1,900

Included with your registration: one full conference registration, one copy of Proceedings CD-ROM, final list of attendees on CD-ROM, exhibit hall admission for two booth personnel; additional booth personnel are welcome at a cost of \$50 per person.

For more information visit:

www.imaps.org/devicepackaging or contact IMAPS at 202-548-4001

Exhibitors on the Device Packaging 2005 Proceedings CD-ROM

IMAPS will provide all exhibitors an opportunity to provide up to ten (10) pages of company products, services and contact information to be included on the Conference Proceedings CD-ROM. These CD-ROMs are provided to all technical conference attendees and are for sale through IMAPS to all industry professionals.

This unique feature will promote the Exhibitor's products and abilities much longer than just the Conference. There is a charge of \$50 for this optional feature. This equates to 10 pages of advertising for just \$50.

These submissions must be no more than ten (10) pages long and must be sent, electronically, in Word or PDF format, to abell@imaps.org no later than February 18, 2005.

Monday continues

SESSION 2: DESIGN/MODELING

Chairs: Christo Bojkov, Texas Instruments;
R. Wayne, Johnson, Auburn University
2 pm – 5:25 pm

Superior Electrical Properties of High Performance Glass Ceramic Packaging for Demanding SiGe, ASIC, Microprocessor and Advanced Server Applications
Warren D. Dyckman, Benjamin Fasano, Christopher Spring, Gary LaFontant, IBM

Controlling Simultaneous Switching Noise with Built-in Bypass Capacitors
Narimasa Takahashi, IBM

Leading Edge Clearance Effects on Natural Convection in Parallel Plate and Finned Metal Foam Heat Sinks
Anandaroop Bhattacharya, R. L. Mahajan, Indian Institute of Technology, Bombay

SESSION 3: WAFER BUMPING

Chairs: Peter Elenius, E&G Technology Partners LLC;
Jamin Ling, Kulicke & Soffa Industries Inc.
2 pm – 5:25 pm

Stress in Thin Films - Fundamentals and Applications in WL CSP
Christo Bojkov, Texas Instruments

Gold Bump Technologies - Plating versus Ball Bumping
Daniel D. Evans, Palomar Technologies

Stud Bumping for Flip Chip - An Alternative Strategy
Jamin Ling, Matt Meyer, Matt Osborne, Vincent McTaggart, Kulicke & Soffa Industries Inc.

Break in Exhibit Hall: 3:15 pm – 3:45 pm

Buoyancy Induced Convection in Metal Foam and Finned Metal Foam Heat Sinks
Anandaroop Bhattacharya, R. L. Mahajan, Indian Institute of Technology, Bombay

Layer Count Reduction for Area Array Escape Routing
Rui Shi, Hongyu Chen, Chung-Kuan Cheng, University of California

Evaluation of the High Frequency Transmission Properties of the Fine Wiring Packaging Substrates Based on the 3D Electromagnetic Simulation
Masataka Yamaguchi, Satoru Kuramochi, Yoshitaka Fukuoka, Dai Nippon Printing Co., Ltd.

High-Speed Electrical Performance of Multi-Row Lead Frame Packages
Sam Karikalan, STATS ChipPAC, Inc.

Factors Limiting the Electrodeposition Rate of Various Bumps for Flip Chip Interconnects
Bioh Kim, Bob Batz, Tom Ritzdorf, Semitool, Inc.

Flip Chip Bonding Enabled by Ink Jet Printing of UBM, Solder Bumps and Underfill
Donald J. Hayes, MicroFab Technologies, Inc.

Advances in Resist Processing and Alignment Technology for Wafer Level Packaging
Chad Brubaker, Markus Wimplinger, EV Group, Inc.

Land Grid Array (LGA) as a Pb-Free Approach for Ceramic Ball Grid Array Packages
Linda Bal, Terry Burnette, Thomas Koschmieder, Joachim Rayos, Freescale Semiconductor

Reception in Exhibit Hall: 5:30 pm

Conference Proceedings CD-ROM	Conference Hotel
<p>If you are unable to attend the Conference and would like a copy of the Proceedings CD-ROM, you may purchase a copy by using the registration form. Your copy will be mailed to you after the event.</p> <p>The cost is \$100 for members; \$175 for nonmembers,* plus shipping and handling. Reserve your copy on-line at www.imaps.org/devicepackaging or call 202-548-4001.</p>	<p>HILTON SCOTTSDALE RESORT & VILLAS 6333 NORTH SCOTTSDALE ROAD SCOTTSDALE, AZ 85250-5428 PHONE: 480-948-7750</p> <p>Single/Double \$169 <i>Please reference IMAPS when making reservation.</i></p> <p>Hotel Discount Ends: February 1, 2005</p>

Tuesday, March 15

Registration: 7:30 am – 5 pm

Continental Breakfast: 7:30 am

Exhibit Hours: 9 am – 5 pm

SESSION 4: MEMS

Chairs: Daniel Baldwin, Engent, Inc.;
Leonard Schaper, University of Arkansas
8 am – 11:25 am

Open-Cavity IC Plastic Packages: Supporting Today's Challenges for the Selection of the Ideal Production Package

David Hynarowski, Ellen Emery, Bill Lawrence, Bob Blue, Quik-Pak, Division of Delphon Industries

Active Micromachined Vibration Isolation Filters using Electrostatic Actuation to Enhance Packaging for Mechanically Harsh Environments

Robert Dean, Ken MacAllister, Nicole Sanders, Scotte Hodel, George Flowers, R. Wayne Johnson, Auburn University; Mike Kranz, Morgan Research Corporation

Magnetics on Silicon using Electroplated Magnetics Materials

Sean Cian O'Mathuna, Terence O'Donnell, Saibal Roy, NingNing Wang, Paul McCloskey, Andrew Connell, NMRC

SESSION 5: MATERIALS

Chairs: Scott Cummings, Dow Chemical Co.;
Beth Keser, Freescale Semiconductor
8 am – 11:25 am

A Hermetic Liquid Crystal Polymer Printed Circuit Board Based Packaging Platform for Highly Integrated Devices
Linus Jauniskis, Brian Farrell, Foster-Miller, Inc.

High Performance UV Curing Adhesive for Image Sensor Package

Yukinari Abe, Osamu Suzuki, Yuuka Soya, Junich Kaneko, Namics Corporation

Lead Zirconate Titanate Thin Films Directly on Copper Electrodes for Embedded Passive Applications

Sudarsan Srinivasan, Angus I. Kingon, North Carolina State University

Break in Exhibit Hall: 9:15 am – 9:45 am

Near Hermetic Liquid Crystal Polymer Air Cavity Packaging for Microwave, MEMS and Optical Applications

John W. Roman, RJR Polymers, Incorporated

Development and Characterization of Transmission Laser Bonding Technique

Jong-Seung Park, Ampere A. Tseng, Arizona State University

3-D Microsensor Modules for Future Intelligent Environments

Bivragh Majeed, John Barton, Kieran Delaney, Stephen Bellis, Kafil Mahmood, Brendan O'Flynn, Bivragh Majeed, Andrew Lynch, Sean Cian O'Mathuna, NMRC

Sloped Sidewall DRIE Process Development for Through Silicon Vias

Swetha Polamreddy, R. Figueroa, S. Burkett, S. Spiesshoefer, L. Schaper, University of Arkansas

Impact of Material Properties and Assembly Geometry on Bond-line Stress When Bonding PCBs to Heat Sinks with an Isotropic Conductive Adhesive

Andrew P. Collins, Emerson and Cuming

Stress Control in Thin Wafers for Backside Metal Applications

Kathy O'Donnell, N. Brings, J. Chiu, J. Kostetsky, S. Golovato, D. Goodman, NEXX Systems Inc.

Low Temperature Curing of Polymer Films for Wafer Level Packaging

Robert L. Hubbard, Lambda Technologies, Inc.

Processing and Reliability of No Flow Underfills and the Influence of Underfill Voids

Dan Baldwin, Engent, Inc.

Lunch in Exhibit Hall: 11:30 am – 12:30 pm

SESSION 6: SiP/3D PACKAGING

Chairs: Flynn Carson, ChipPAC, Incorporated;
R. Wayne, Johnson, Auburn University
1 pm – 4:25 pm

A Novel MEMS Based Ultra-High Density Interconnect for Wafer-Level Ultra-Thin Die Stacking Technology
Parthiban Arunasalam, Harold D. Ackler, Sandeep Makhar, Bahgat G. Sammakia, State University of New York at Binghamton

Electrical Performance Limitations of On-Package Decoupling Capacitors
Leonard W. Schaper, Richard K. Ulrich, University of Arkansas

Flexible and Embedded Packaging of Thinned Silicon Chip
Kyu-Ho Shin, Chang-Ryoul Moon, Tae-Hee Lee, Yong-Jun Kim, Samsung Advanced Institute of Technology

SESSION 7: OPTOELECTRONICS

Chairs: Michael Toepper, Fraunhofer IZM;
Gilbert Lecarpentier, SUSS MicroTec
1 pm – 4:25 pm

Low Outgassing Materials for Electro-optic and Electronic Systems
Bill Riegler, Stephen Bruner, Rob Thomaier, NuSil Technology

Transparent Combo-Lids® for Sensors and Communication
Heiner Lichtenberger, Michael J. Zasowski, Gery Lovitz, Joseph J. Alfano, Williams Advanced Materials

Fiber-Waveguide Base Optical Subassembly with Polymer Optical Bench
Ming-Lang Tsai, Ming-Jie Chou, Wen-Shan Lin, Jin-Sheng Chang, Yii-Tay Chiou, Chun-Hsun Chu, Industrial Technology Research Institute

Break in Exhibit Hall: 2:15 pm – 2:45 pm

Advances in the Implementation of Embedded Passives in Low Temperature Co-Fired Ceramic Packages
Christopher R. Needes, Daniel I Amey, K. Mani Nair, DuPont Company

SoP Design on Liquid Crystal Polymer Substrate for 5GHz RF Receiver Front-End Module
Yasar Amin, University of Engineering and Technology Taxila; Li-Rong Zheng, Hannu Tenhunen, Xinzhong Duo, Royal Institute of Technology (KTH)

3D Package Innovations for Enabling System Level Integration and Miniaturization
Vern Solberg, Tessera, Inc.

Choosing the Right “Stacked” Memory-Packaging Architecture for Today’s Microelectronics Applications
David P. Sempek, Amkor Technology, Inc.

Au-Sn Solder Electroplating for Microelectronic/Optoelectronic Packaging
Siamak Akhlaghi, Doug Ivey, Micralyne Inc.

Using Six Dimensional Force Feedback for Precision Optoelectronics Alignment, Attach, and Re-Align
Andre By, Automation Engineering Incorporated

Index Matching Silicone for High Brightness LED Packaging
Bill Riegler, Rob Thomaier, NuSil Technology; Randall Elgin, Lightspan Application Lab.

Device Packaging at Sub-Micron Accuracy Applied to an Optical Silicon Bench at Sub-Micron Accuracy
Gilbert Lecarpentier, SUSS MicroTec; Bertrand Paris, Stéphane Rabaron, Avanex France

Reception in Exhibit Hall: 4:30 pm

Travel



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Wednesday, March 16

Registration: 7:30 am – 12:15 pm

Continental Breakfast: 7:30 am

SESSION 8: PROCESS TECHNOLOGY

Chairs: Kathy O'Donnell, NEXX Systems Inc.;
Robert Hubbard, Lambda Technologies, Inc.
8 am – 12:15 pm

Micro Laser Welding of Thin Metals in Circuit Interconnections

Ron Mundt, Gary O'Dell, Mundt & Associates

Pad Oxide Growth during Wafer Singulation

Jerry White, Freescale Semiconductor

Package Assembly and Reliability Impacts Associated with Fine Pitch/Small Bond Pad, Circuit under Pad and Multiple Probe Marked Die

Simeon K. Iliev, SMSC

SESSION 9: FLIP CHIP PACKAGING

Chairs: Jon Aday, Amkor Technology Inc.;
Sean Cian O'Mathuna, NMRC
8 am – 12:15 pm

Wireability Comparison of Flip Chip Substrates as a Function of Chip Design and Substrate Capability

Irving Memis, Endicott Interconnect

Understanding and Optimizing Thermal Interface Materials for High Performance Flip Chip Devices

Chris Lee, Greg Becker, Dow Corning

Board Strain States Method and FCBGA Mechanical Shock Analysis

Frank Z. Liang, Richard L. Williams, George Hsieh, Intel Corporation

Break: 10:30 am – 10:45 am

Wire Bonding to Stack Die, Automotive and Optoelectronic Packaging: Different End Application with the Same Challenges

Kevin M. Seufert, Unaxis USA - Assembly and Packaging (ESEC)

Enhancement of Solder Ball Bumping Process for RF-MEMS Packaging based on Surface Conditions

Arthur Darbinian, K. H. Shin, C. Y. Moon, J. H. Lim, Samsung Advanced Institute of Technology

100 Newton Ultrasonic Bond Head for Flip Chip Device Bonding

Philip Coutts, Tsunehisa Nishioke, Motoyuki Kawahara, TDK Corporation of America

Direct Write Micro-Printing Technology: An Enabler for Opto-Electronic Packaging

Donald J. Hayes, Ting Chen, MicroFab Technologies, Inc.

Successful Implementation of Plasma Processing for Flip Chip Underfill Applications

James D. Getty, Jack Zhao, Hirotaka Tanabe, March Plasma Systems

The Effect of Thermal Aging above the Underfill Glass Transition Temperature on Organic Flip Chip Package Reliability

Jason P. Goodelle, Charles Cohn, Christopher Horvath, Weidong Xie, Agere Systems

The Effect of Drill Hole Quality on Via to Via Isolation in Organic Flip Chip BGA Substrates

Charles Cohn, Barry J. Dutt, Jason P. Goodelle, Ronald J. Weacheck, Agere Systems

A Comparative Study of BGA Solder Joint Reliability under Four-Point Bend and Spherical Bend

Phil Geng, Mitul Modi, Carolyn McCormick, Alan McAllister, Arnaldo Nazario, Intel Corporation

Mark Your Calendar....

Passive Integration

Marco Island, Florida

January 24 - 26, 2005

www.imaps.org/passives

Reliability of Advanced Electronic Packages and Devices in Extreme Cold Environments

Pasadena, California

February 21 - 23, 2005

www.imaps.org/extremecold

Ceramic Interconnect and Ceramic Microsystems Technologies Conference (CICMT)

Baltimore, MD

April 10 - 13, 2005

www.cicmt.org

Military, Aerospace, Space and Homeland Security: Packaging Issues and Applications May 2005

www.imaps.org/military

FOLLOWING THE DEVICE PACKAGING CONFERENCE....

Global Business Council (GBC) - Winter Conference 2005

Addressing the Business Side of Microelectronics
(Formerly the Microelectronics Market Research Council or MMRC)

The Business of Device Packaging and 2005 Industry Forecast

March 16 - 17, 2005

Hilton Scottsdale Resort & Villas

(Co-located with IMAPS International Conference and Exhibition on Device Packaging, March 13-16, 2005)

Wednesday March 16, 2005

7:00 AM: GBC Golf Tournament
Sanctuary Golf Course, Scottsdale, AZ

3:00 PM: Registration Begins

5:30 PM: Welcome Reception

6:30 PM: Keynote Session
Todd Bankofier, President and CEO
Arizona Technology Council and Member of Arizona Governor's Council
on Innovation and Technology

Thursday March 17, 2005

7:00 AM: Registration

7:30 AM: Continental Breakfast

8:00 AM: Opening Remarks
Michael O'Neill, GBC Steering Committee Chair

Session 1: The Business of Device Packaging

Session Chair: Mike O'Neill, Heraeus Inc.,
CMD

8:10 AM: Ceramics: A Case for a Business
Doug Russell, Natel Engineering

8:55 AM: Overcoming the Hurdles to RF SiP
Joseph Adams, Skyworks Inc.

9:40 AM: Break

10:00 AM: TBD
Steve Greathouse, Intel

Session 2: 2005 Microelectronics Market Forecast

Session Chair: George Toskey, Dow
Corning

10:45 AM: TBD
Jim Walker, Gartner – Dataquest

11:30 AM: Where Do Semiconductors Go from Here: New Markets
Morry Marshall, SEMICO

12:15 PM: Lunch

1:30 PM: Updated Global Semiconductor Forecast
Bill McClean, IC Insights

Session 3: 2005 Microelectronics Industry Financial Outlook

Session Chair: Laurie Roth, K&S

2:15 PM: Impact of Off-Shoring and the Sub-Con Business Model
Bill Lu, Piper Jaffray & Co.

3:00 PM: Break

3:20 PM: Industry Update
Timothy Arcuri, Smith Barney

4:05 PM: Technologies Worth Investing In - How Does Wall Street Decide Where to Place its Bets
Brett Hodess, Merrill Lynch

4:55 PM: Panel Discussion

6:00 PM: Closing Remarks and Adjourn

7:00 PM: GBC Wild West St. Patty's Day Dinner
Rawhide Western Town and Steakhouse
(Bus Departs 6:40)

Visit www.imaps.org/gbc for registration information.

Announcement & Call for Abstracts IMAPS Topical Workshop & Exhibition on Flip Chip Technologies

Marriott Austin at the Capitol
Austin, Texas USA
June 20 - 23, 2005

Sponsored by
International Microelectronics And Packaging Society (IMAPS)
Everything in electronics between the chip and the system!

Abstract Deadline: February 15, 2005

General Chair:
Andrew J.G. Strandjord, IC Interconnect
Colorado Springs, CO 80907
P: 719-533-1030 ext:13
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Technical Program Co-Chairs:

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Chandler, AZ 85248
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jaday@amkor.com

Ted Tessier, ST Assembly Test Services Inc.
Tempe, AZ 85284
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The International Microelectronics And Packaging Society (IMAPS) is sponsoring its Topical Workshop (TW) on Flip Chip Technologies, to be held June 20-23, 2005, at the Marriott Austin at the Capitol Hotel in Austin, Texas. This meeting is a continuation of the annual Flip Chip Workshop, now in its tenth year and showcases the latest developments in flip chip technology.

As in past years, the technical program will focus on leading edge advances in flip chip technology with particular focus in 2005 on the challenges of flip chip for Cu/Low-K, Pb-free (Green applications), new technologies, and lower cost. The national organization will hold a focused exhibition for suppliers who support the use of flip chip technology.

Abstracts are being requested for the following Flip Chip topics:

- Bumping materials and processes
- Design for flip chip advancements
- Substrate design for flip chip devices
- Substrates and board technology
- Testing of flip chip devices, including KGD and wafer level burn-in
- Assembly processes and assembly issues
- Underfill materials including Wafer Applied Underfills
- Pb-free / Green flip chip bumping
- Cu-Low K packaging considerations
- Non-solder based flip chips
- Reliability
- Thermo-mechanical modeling
- End use applications (i.e., OEM products)

An outstanding program is planned with internationally recognized authorities from industry and academia. **Those wishing to present papers may submit a 200-300 word abstract electronically no later than February 15, 2005. Abstracts should be submitted to the on-line submittal form at: www.imaps.org/abstracts.htm.**

If you are having problems with the on-line submittal form, please email Jackki Morris-Joyner (jmorris@imaps.org) or call 305-382-8433.

Speakers are required to pay a reduced registration fee.

All authors are requested to attend the entire Workshop to maximize opportunities for interaction with registered attendees. This IMAPS Workshop format is a proven forum for effective industry networking.

IMAPS 2005 - Call for Papers

Everything in electronics between the chip and the system!

The 38th International Symposium on Microelectronics will be held at the Philadelphia Convention Center, Philadelphia, PA; September 25 - 29, 2005. It is sponsored by the International Microelectronics And Packaging Society (IMAPS). The IMAPS Technical Committee seeks original papers that demonstrate how new technologies and applications are expanding and redefining microelectronics "between the chip and the system." All abstracts submitted must represent original, previously unpublished work.



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MICROELECTRONIC DEVICES & BACKEND WAFER FAB	1ST LEVEL TECHNOLOGIES AND PACKAGES (SINGLE CHIP & MULTI-CHIP)	2ND LEVEL PACKAGING (BOARD LEVEL)	SYSTEM LEVEL PACKAGING (BOX OR PRODUCT-LEVEL)
<ul style="list-style-type: none">• High Frequency Devices• High Reliability Devices (Military & Aerospace)• MEMS• Optical Devices• Passives• Sensors• Wafer Level Packages• Organic Semi-conductors• Bumping• Cu Metallurgy• Low-K Dielectrics	<ul style="list-style-type: none">• Cu Metallurgy• Die Attach• Flip Chip• Leadframes• Low-K Dielectrics• Molding Materials• Mold Design• Solders• Stacked Die• Substrates (Ceramic, LTCC, PWB, Flex)• Thick and Thin Film Circuit Materials• Integrated Passives• Wirebonding• Thermal Design• Electrical Design• Reliability• CAD & CAE• Area Array Packaging• Thermal Interface Materials• Thermal Packaging• Chip Packaging	<ul style="list-style-type: none">• LED Packaging• MEMS Packaging• Multi-chip Package• Optoelectronics Packaging• Power Packaging• RF/Microwave Packaging• SiP <ul style="list-style-type: none">• Assembly Processes• Embedded Passives• Flex Circuits• PWB• Thin & Thick Film Systems• Encapsulation and Underfill Materials & Processes• Optronics Device Interconnect, Packages & Connectors• Solders• CAD & CAE• Electrical Design• Mechanical Design• Thermal Design• Reliability	<ul style="list-style-type: none">• Connectors• Electrical Design• EMI• Mechanical Design• Thermal Design• Reliability• Safety• Backplanes• Military Packaging• Medical Electronics Packaging• Power Packaging• System Level Test Technology, Equipment & Processes• Optronics Packages & Connectors
Cash Awards Offered! <ul style="list-style-type: none">• Best Paper of the Symposium One (1) \$2000 Cash Award• Outstanding Paper Two (2) \$500 Cash Awards <i>Top 5 considered for Best of Symposium and Outstanding Papers.</i>			
		POSTER SESSION Outstanding papers that do not fit in created sessions will be considered for exposition in the poster session.	

Please send your 250-300 word abstract **electronically only** by February 4, 2005, using the On-line submittal form at:
www.imaps.org/abstracts.htm

Abstract Cut-off Date: February 4, 2005 Notice of Acceptance: April 8, 2005 Final Manuscripts Due: July 30, 2005

All Speakers are required to pay a reduced registration fee.

If you are having problems with the on-line submittal form, please email Jackki Morris-Joyner jmorris@imaps.org or call 305-382-8433.

See You in Philadelphia, Pennsylvania • September 25 - 29, 2005

REGISTRATION FORM

REGISTER ON-LINE AT WWW.IMAPS.ORG/DEVICEPACKAGING
DEVICE PACKAGING CONFERENCE - MARCH 13 - 16, 2005

Dr. Mr. Ms. Member ID# _____
First Name _____ M.I. _____ Last Name _____
Company/Affiliation _____ Job Position _____
Address _____
City _____ State _____ Zip _____ Country _____
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REGISTRATION FEES: EARLY REGISTRATION ENDS 2/1/05

CONFERENCE FEES

(On or before 2/1) (After 2/1)

- | | | |
|---|-------|-------|
| <input type="checkbox"/> Member (IMAPS) | \$515 | \$615 |
| <input type="checkbox"/> Non-Member* | \$615 | \$715 |
| *Includes one-year individual membership in IMAPS | | |
| <input type="checkbox"/> Speaker/Chair | \$300 | \$400 |
| <input type="checkbox"/> Exhibits Only | \$10 | \$10 |

Conference Fee includes one CD-ROM Proceeding and all meals stated in this program.

PROFESSIONAL DEVELOPMENT COURSES* - 1/2 DAY

- | | | |
|--|-------|-------|
| <input type="checkbox"/> Thermal Management Materials - PDC1 | \$300 | \$350 |
| <input type="checkbox"/> Flip Chip Assembly - PDC2 | \$300 | \$350 |
| <input type="checkbox"/> Hermeticity Testing.... - PDC3 | \$300 | \$350 |

*Sunday, March 13: 1 pm - 5 pm

ADDITIONAL PURCHASES

- | | | |
|--|-------|-------|
| <input type="checkbox"/> Guest/Family Member (meals only) | \$150 | \$150 |
| <input type="checkbox"/> CD of Presentations (Member Rate) | \$100 | \$100 |
| <input type="checkbox"/> CD of Presentations (Non-Member Rate) | \$175 | \$175 |
| <input type="checkbox"/> Add to Ship in the US | \$7 | \$7 |
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EXHIBIT BOOTH (DEADLINE: FEBRUARY 1, 2005)

- | | | |
|--|---------|---------|
| <input type="checkbox"/> IMAPS Corporate Member | \$1,100 | \$1,300 |
| <input type="checkbox"/> Non-IMAPS Corporate Members | \$1,700 | \$1,900 |
| <input type="checkbox"/> Yes, we will participate in the CD-ROM* | \$50 | |

*see inside for details and deadlines.

Booth fee includes, one full conference registration, one copy of the Proceedings CD-ROM, final list of attendees on CD-ROM, exhibit hall admission for two booth personnel; additional booth personnel are welcome at a cost of \$50 per person.

HOUSING (Hotel Cut-off is February 1, 2005)

Housing Accommodations **must** be made directly to:

Hilton Scottsdale Resort & Villas
6333 North Scottsdale Road
Scottsdale, AZ 85250
Ph: 480-948-7750

Single/Double - \$169

Please reference IMAPS when making reservations.

PAYMENT

Conference Fee: \$ _____
Professional Course: \$ _____
Additional Purchase: \$ _____
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Total Payment Due: \$ _____

- Enclosed is a check payable in US funds to IMAPS
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Wire Transfer information can be found on-line at

www.imaps.org/registration/devicepackaging.asp

Mail this form with payment to: IMAPS * 611 2nd Street, NE * Washington, DC 20002-4909. For credit card transactions, register on-line: www.imaps.org; or register by phone with your credit card by calling 202-548-4001; Fax: 202-548-6115. Additional information? E-mail: IMAPS@imaps.org, or visit our web site: <http://www.imaps.org>. Cancellations will be refunded (less a \$50 processing fee) only if written notice is postmarked on or before **Friday, February 25, 2005**. No refunds will be issued after that date.

IMAPS Registration

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