Program, Exhibition and Registration Information
www.imaps2001.org

Bursting With Innovation

Advance Program And Registration

34th International Symposium on Microelectronics

IMAPS

October 9–11, 2001
Baltimore Maryland

EXHIBITION:
October 9-11, 2001
at the
BALTIMORE CONVENTION CENTER

CONFERENCE & EVENTS:
October 7-11, 2001
FEATURING:
- 21 Technical Sessions
- Special Poster Session
- 20 Professional Development Courses
- 3 “Hands-on” Factory Training Workshops
- Special Plenary Session

message

FROM THE GENERAL CHAIR

You are cordially invited to attend the 34th IMAPS International Symposium and Exhibition on Microelectronics! Plan to attend this signature event of the Society. The IMAPS 2001 Steering Committee and the Capital Chapter members look forward to sharing with you a program that we hope will exceed your expectations.

The Technical Program will commence with Professional Development Courses (PDCs). We have retained many of the excellent courses offered at IMAPS '00 in Boston. We are also offering several new PDCs. It is our intent to cover a broad spectrum of microelectronics technology with this part of the Technical Program.

The Welcome Reception will again provide a pleasant location where we can meet old friends and make new ones in an atmosphere conducive to relaxation and conversation.

The Technical Program will continue with a Plenary Session just as we had in 1989—the last time the show was in Baltimore (and what a fine time we had then!). One of the purposes of the Plenary Session is to lend an atmosphere of cohesiveness to the rest of the Technical Program. This year we will include the Awards Ceremony as a part of the Plenary Session. We hope you will join us to honor our deserving Award recipients.

Following the PDCs, we will present a Symposium that has been designed to maximize your opportunity to gain knowledge in many areas of advanced microelectronics technology. We are fortunate to work in a field that drives a significant and increasing portion of the industrial world's economy. Full Symposium attendees will have the opportunity to dialog with our colleagues who are driving these advances.

As a result of the strong show in Boston last year, we stand a good chance of selling out the Exhibition Hall early. If you haven't yet registered as an Exhibitor, now is the time! The Exhibits will be located in one large area directly below the rooms where the Technical Program will be presented. Lunch will again be served two days in the Exhibition Hall and an "Octoberfest" late afternoon reception will be held there as well. Attendees who engage many of the Exhibitors will see that the products and services proudly presented are the engine that drives the technology presented at the Symposium.

Review this brochure carefully to learn more about the show features described previously as well as the Education Program, the Silent Auction, opportunities for Sponsorship, the Golf Tournament, and the Spouse/Guest Program.

Don't forget to check out the web site devoted specifically to the show: www.imaps2001.org for the latest information and join us for a show that we promise will be "Bursting with Innovation"!

John Graves
Microelectronics Research Laboratory
jgraves@micro-research.org

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2001 Symposium Committee – Baltimore

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Sponsorship Chair:
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Silent Auction Chair:
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Spouse Program Chair:
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IMAPS 2002 General Chair:
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IMAPS Executive Director:
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rb1959@aol.com

What Your 2001 Full Symposium Registration Includes

Your registration includes the Plenary Session, Awards Ceremony, Technical Sessions, Exhibits, Welcome Reception, Exhibit Hall Lunches, 2001 Proceedings (printed & CD-ROM Versions), and an automatic one-year IMAPS membership renewal for individual and student members in good standing at the time of registration. For an additional fee you can register for the Professional Development Courses (PDC), Hands-on Training Workshops, Golf Tournament, and the Spouse/ Guest Program.

IMAPS 2001

Registration Hours

Sunday	Oct. 7	8:00 AM – 4:00 PM
Monday	Oct. 8	8:00 AM – 5:00 PM
Tuesday	Oct. 9	7:00 AM – 6:00 PM
Wednesday	Oct. 10	7:00 AM – 5:00 PM
Thursday	Oct. 11	7:00 AM – Noon

Exhibit Hours

Tuesday	Oct. 9	9:30 AM – 6 PM
Wednesday	Oct. 10	9:00 AM – 5 PM
Thursday	Oct. 11	9:00 AM – Noon

2001 Symposium Committee

imaps 2001

7th Annual IMAPS Golf Classic

to benefit the

IMAPS Educational Foundation

Monday, October 8, 2001

The IMAPS 2001 Golf Classic will be held at Greystone Golf Course in White Hall, Maryland, on Monday, October 8, 2001. The tournament will feature a shotgun start with prizes awarded to the overall winners, as well as those closest to the pin and with the longest drive.

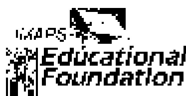
Greystone Golf Course is located in northern Baltimore County on 215 acres of rolling farmland. The course was designed by Joe Lee – golf course architect of Doral's Blue Monster and the magical courses at Walt Disney World in Orlando, Florida. The signature hole on the course is #4, a 152-yard par 3 featuring water in the front and left of the green and an environmentally protected area on the right. The course plays 6,161 yards from the white tees, with five par 5s, of which four are reachable in two. Daring the players on the course is 140 feet of elevation changes, 7 ponds, and 86 bunkers. In addition to the breathtaking scenery on the course, the fresh air of the country surroundings will be a wonderful escape from the big city atmosphere.

Cost is $125 before September 4, 2001, and $150 after and on-site. The cost includes transportation, lunch, greens fees, cart, and the use of the range and practice facilities.

Please Note: Proper golf attire is required. Men's shirts without collars, gym shorts, and jeans are not permitted. The Golf Course also requires that all players wear soft-spiked golf shoes.

Hole sponsorships are available: $350 & $500. Please contact Keith Sellers, 2001 Golf Chair (kmsellers@hotmail.com) or Doug Paul, IMAPS (dpaul@imaps.org) for details.

Hole Sponsors:



Advanced Packaging - Pennwell
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Technic, Inc.
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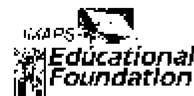


5th Annual IMAPS Educational Foundation Silent Auction

Come one, come all!
Bid-Boards for the 2001 IMAPS Educational Foundation Silent Auction are available for viewing and bidding during these symposium events and hours:

Monday, October 8th
8:00 AM to 5:00 PM, Registration area
Welcome Reception: 6:30 PM to 8:00 PM

Tuesday, October 9th
9:30 AM to 6:00 PM
Wednesday, October 10th
9:00 AM to 4:00 PM
Exhibit Hall on Tuesday and Wednesday

Winning bidders can pay for and pick up items at the Registration Cashier's desk
on
Wednesday, October 10th, from 4:00 PM to 5:00 PM
and
Thursday, October 11th from 9:00 AM to Noon.

Available items must be picked up during these hours.
Donors are responsible for shipping prizes to winning bidders!

Student Program

Reduced Symposium Registration

IMAPS offers students a reduced registration fee for IMAPS 2001. The cost for students to attend the Full Symposium is $10 for Members and $15 for Non-members (before September 4, 2001); $20 for members and $25 for Non-members after the deadline. Your registration includes the Plenary Session, Technical Sessions, Exhibits, Welcome Reception, Exhibit Hall Lunches, 2001 Proceedings (printed & CD-ROM versions) and an automatic one-year IMAPS Membership renewal. IMAPS/NSF is also offering a Special PDC Course (M13) to **students only** free of charge. See page 19 for more details.

Professional Development Course (PDC) Monitors, October 7 - 8, 2001

There will be 23 PDC courses during IMAPS 2001. One monitor will be assigned to each PDC. PDCs are scheduled on Sunday, October 7 and Monday, October 8 and run from 9:00 a.m. to 5:00 p.m. Course monitors assist PDC instructors (distribute handouts, monitor lights, collect evaluations, etc…) and in return may monitor the course at no charge. Monitors will receive free course materials (not including textbooks) and lunch on the day of their PDC offering. PDC monitors will receive no financial compensation. Monitors will be assigned on a first-come, first-served basis. Sign up early to ensure the PDC of your choice. Please email Doug Paul (dpaul@imaps.org) with your top three choices.

Best Student Paper, October 9 – 11, 2001

A review committee will attend all technical presentations by student authors, to evaluate and determine the *Best Student Paper*. The student will be evaluated on presentation skills, audience interaction and technical knowledge. A portion of the credit will be dedicated to the written portion of the manuscript. The winning student will receive a certificate and recognition in *Advancing Microelectronics*.

Student Chapter Booth Competition, Tuesday, October 9, 2001, 9:00 am – 11:00 am

Each student chapter is encouraged to enter a booth and exhibit on the main floor. These booths are free to student chapters and allow chapters to demonstrate their activities to the microelectronics industry. Chapters will be evaluated, by a panel of judges, on various criteria including, but not limited to - general appearance and appeal of the display, diversity of display (curriculum, activities, and projects), knowledge of critical issues with the program offered in the institution, sound technical awareness, eye contact, enthusiasm, appearance, ability to address questions and feedback provision. Recognition will be given to the *Best Student Chapter Booth* at the Student/Industry Reception on Tuesday, October 9, 2001. (Instructions on the booth specifications will be available at a later date.)

Student/Industry Panel, Tuesday, October 9, 2001, 4:00 pm – 5:30 pm

The panel will have invited guests ranging from industry professionals, industry recruiters, to educators describing how their education, interests and career experiences led to their current positions. It will also provide an opportunity for students to learn what industry expectations are and how to start their long-term career development. The panel participants will include George Harman - *NIST*, Dr. David L. Wilcox – *Motorola, Inc.*, Dr. W. Kinzy Jones - *Florida International University*, Dr. Paul Collander - *Nokia Networks*, and Dr. Charles E. Bauer - *TechLead Corporation*. Each panelist will speak for 10 – 15 minutes. Students will then have the ability to participate in a Q & A session with the panelists.

Student/Industry Reception, Tuesday, October 9, 2001, 5:30 pm – 6:30 pm

Students will have a chance to network and talk one-on-one with each other and the panelists. Refreshments will be served. Announcement of *Best Student Chapter Booth* will also take place during the event.

With all this planned for students, it would be a shame if you missed out on the excitement! For more information, please visit the IMAPS webpage – www.imaps2001.org

2000 - 2001
IMAPS Educational Foundation Grant Recipients

Rokan Ahmad
Columbia University

Daniel M. Bennett
Brigham Young University

Jane E. Clayton
Iowa State University

Richard E. Eitel
Penn State

Dean M. Goedde
University of Illinois at Urbana/Champaign

Jeffrey Haeni
Penn State University

Theron Lewis
Iowa State University

James Pyland
Georgia Institute of Technology

David C. Reichenbacher
University of Wisconsin-Madison/Thermal Spray Technologies, Inc.

Jason Sternhagen
South Dakota State University

Lejun Wang
Georgia Institute of Technology

imaps 2001

We Are Bursting with Excitement to See You at the IMAPS 2001 Welcome Reception!

At 7 a.m. on the morning of September 13, 1814, the British bombardment of Ft. McHenry began. A 30 by 42 ft. flag that the British would have no trouble seeing flew proudly, ready to face the enemy. The bombardment continued for 25 hours, the British firing 1,500 bombshells that weighed as much as 220 pounds each and carried lit fuses that would supposedly cause them to explode when they reached their targets. However, the bombshells weren't very dependable and often burst in mid air. From special small boats, the British fired the new Congreve rockets that traced wobbly arcs of red flame across the sky. That evening, the cannonading stopped, but at about 1 a.m. on the 14th, the British fleet roared to life, lighting the rainy night sky once again with their ordnance.

Francis Scott Key, a respected young lawyer from Baltimore, watched the battle with apprehension. He knew that as long as the shelling continued, Fort McHenry had not surrendered. However, long before daylight there came a sudden and mysterious silence. What Key did not know was that the British land assault on Baltimore as well as the direct naval attack, had been abandoned. Judging Baltimore as being too costly a prize, the British officers had ordered a retreat.

In the predawn darkness, Key waited for the sight that would end his anxiety—that of Ft. McHenry's great flag blowing in the breeze. When at last daylight came; the flag was still there! The experience inspired Key to pen the poem which later became our National Anthem.

Baltimore, the city that inspired our country's national anthem, is looking forward to welcoming you to IMAPS 2001, the 34th International Symposium on Microelectronics. We are particularly proud to welcome our international guests and encourage everyone to enjoy the many historical and cultural attractions that Baltimore has to offer including Ft. McHenry. The early Fall weather should offer a pleasing climate and colorful palette for all activities.

Please join us at this year's Welcome Reception as we prepare to celebrate the technological advances that are bursting upon the microelectronics scene. You will be able to enjoy an evening of excellent food and refreshments, meet friends and colleagues, make new acquaintances, and carry on quiet conversations in an atmosphere that we promise will be low-Key!

We Are Bursting with Excitement to See You at the IMAPS 2001 Welcome Reception!

Welcome Reception

Monday, October 8
at the
The Hyatt Regency Baltimore
6:30 – 8:00 PM

Sponsored by:

Heraeus, Inc. / Circuit Materials Division

Spouse/Guest Program

Tuesday, October 9, 2001
9 AM - 4:30 PM

Welcome to Baltimore! Today you will visit the vibrant harbor city of Baltimore, the home of Edgar Allan Poe, the Baltimore Orioles, the Super Bowl Champion Baltimore Ravens and the "Star Spangled Banner."

After a brief riding tour past Johns Hopkins University and Baltimore's residential neighborhoods, you will visit **Evergreen House**, a magnificent Italianate mansion situated on 26 lush acres. Evergreen House was the home of the founders of the B & O Railroad, the Garrett family, who lived at Evergreen from 1878 to 1952. Recently restored, this opulent mansion is listed on the National Register of Historic Places. Complete with Theatre Wing and Rare Book Library, this forty-eight-room Classical Revival structure houses a significant collection of American, European and Oriental fine and decorative art.

You will then continue on to the **Baltimore Museum of Art** - Unique, elegant and sophisticated, this is Maryland's largest art museum. The BMA is home to more than 100,000 objects ranging from antiquity to present. *The Cone Collection* — The Baltimore Museum of Art's remarkable holdings of Post-Impressionist and modern art — is the cornerstone of the Museum's permanent collection. The highlight is a group of 500 works by Henri Matisse, considered among the most important and comprehensive of its kind in the world. Major examples by Pablo Picasso, Paul Cezanne, Paul Gauguin, Vincent van Gogh, Pierre-Auguste Renoir, and other icons of early 20th century French art are also included.

You will drive through the neighborhoods of **Little Italy and Fells Point** and stop for lunch at Sabatino's, before visiting the **National Aquarium**, home to over 5,000 aquatic animals, including sharks, whales and seals. At the Aquarium you can explore diverse habitats from a frosty Icelandic coast to a steamy tropical rain forest. Find yourself surrounded by an Atlantic coral reef, hundreds of tropical fish, or several varieties of ferocious looking sharks. The highlight of your visit will be the **dolphin show** in the Marine Mammal Pavilion. Voted one of the premier aquariums in the world, the National Aquarium is sure to fascinate and delight all. We will return to the hotel at approximately 4:30 p.m.

Wednesday, October 10, 2001
9 AM - 5:30 PM

A Day on the Eastern Shore. You will enjoy one of the most amazing waterways in the United States. Your journey includes a well-versed Tour Guide to entertain you along the way. First stop will be historic Annapolis, Maryland. Led by a guide in colonial dress, you'll begin with a walking tour of the US Naval Academy where you can amble across the Quad and through the Navy Chapel then into the crypt of Naval hero John Paul Jones.

Then it is onwards to the Eastern Shore. Guests will enjoy refreshments on their journey across the Bay Bridge and on to St. Michaels. Once in St. Michaels guests will be treated to a delightful luncheon on the Eastern Shore at the Oaks, where you will be treated like royalty in a private secluded setting. The Oaks is a place where history and beauty are neighbors. Built in 1748 as a private residence, this Talbot County manor house is a showcase of structural renewal. The facade retains its antebellum geniality and grace, but the entire Inn has been renovated with your comfort and ease in mind. At the turn of the century, guests arrived by steamship or train to enjoy the bounty and tradition of Maryland's Eastern Shore.

After lunch you will enjoy the town of St. Michaels for shopping and browsing. We will return to the hotel at approximately 5:30 p.m.

Tuesday only: $90 – Advance; $120 – On-site
Wednesday only: $120 – Advance; $175 – On-site
2-Day Package: $190 – Advance; $220 – On-site

**Please note that lunch is included on both days. No breakfast will be provided.*

A Special Thank You...

EP&P magazine has agreed to send a special IMAPS 2001 brochure with its August issue to the magazine's East Coast mailing list.

IMAPS Organizational Member, MRSI, has agreed to fund the development and printing of the brochure.

Many thanks to MRSI!

hands-on workshops

The hands-on workshops sell out quickly and enrollment is limited, please check for availability.

Sunday, October 7
9 am - 5 pm

The "hands-on" courses are back! Last year the "hands-on" courses sold out early and were an overwhelming success. IMAPS, in partnership with the National Training Center for Microelectronics (NTCμ) is again offering technical training sessions designed to provide attendees with a "hands-on" learning experience. Enroll early as class size is limited!

S1

Wirebonding (how to) for Operators and Technicians

Enrollment limited to 12 students

Instructor: Thomas J. Green, National Training Center for Microelectronics

Workshop Summary:

This course is intended as a practical "hands-on" set of laboratory exercises to allow the operators to really understand the wirebonding process. An experienced industry instructor will review the basic manual wirebonder equipment design and setup and explore how machine settings such as power, time, force and stage temperature affect the bonding process. Both ultrasonic wedge and thermosonic ball bonding will be explored using the industry's latest manual wirebonders. Students will also have an opportunity to perform wire pull and ball shear testing and visually inspect wirebond interconnects to gain further insights into the process.

Benefits:

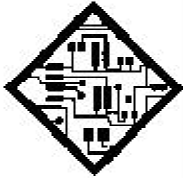
- Understand the basics of thermosonic and ultrasonic wire bonding.
- Recognize visual defects and how to prevent them.
- Learn how to do wire pull and ball shear testing.
- Know how to set up and use manual wirebonding equipment.

Who Should Attend:

This course is intended as a beginning to intermediate level course for operators, technicians and others with limited wire bonding experience interested in a practical "hands-on" tutorial.

Tom Green has eighteen years experience in the microelectronics industry and presently teaches at the National Training Center for Microelectronics. As a staff engineer with Lockheed Martin he was responsible for the materials and processes used in building custom hybrids and RF microcircuits for space applications. Specific areas of expertise included wirebonding, die attach and seam sealing. As an officer assigned to USAF Rome Laboratories he conducted research on semiconductor failure mechanisms and analyzed numerous microelectronic component failures from Air Force avionics systems. He has published seven technical papers and is a member of the IMAPS National Technical Committee. Tom earned a B.S. in Metallurgy and Materials Engineering from Lehigh University and a Masters in Engineering from University of Utah.

NTCμ hands-on factory training workshops



The National Training Center for Microelectronics (NTCμ), located in Bethlehem, Pennsylvania, is an extension of Northampton Community College. NTCμ is the recognized leader in microelectronics manufacturing industry training and is known for clear, concise "hands-on" training courses specializing in hybrid, RF and related technologies. All courses carry Continuing Education Units (CEU) which earn credit toward your degree. Website: www.northampton.edu/ntc.

S2

Screen Printing (how to) for Operators and Technicians

Enrollment limited to 10 students

Instructor: David Malanga, Heraeus, Inc., Circuit Materials Division

Workshop Summary:

This course is designed to focus on the concepts of screen printing and firing of thick film materials. An overview of the screen printing process will be given with a "hands-on" demonstration to emphasize printer set up and operation. Screen print process parameters such as snap off, pressure and print speed and how they effect the finished print will be explored in detailed. Each student will have an opportunity to print various types of thick film materials using a variety of different screens. State-of-the-art microscopes and thickness profiling equipment will be available to assess the quality of the wet print. The firing process and its effect on the finished print will be discussed in detail.

Benefits:

- Understand the importance of proper screen printer set up.
- Learn to trouble-shoot screening problems.
- Understand the factors that affect wet print thickness and line resolution.
- Understand the issues with proper furnace set up and atmospheric control.

Who Should Attend:

The course is intended for operators and technicians and others who need to gain a deeper understanding of the thick film printing process.

David Malanga is currently Technical Service Manager for Thick Film Products at Heraeus Inc., Circuit Materials Division. Dave has eleven years at Heraeus working both in R&D formulating materials (resistors, conductors, and dielectrics) and in Technical Service solving processing and application problems directly with customers. Dave earned a B.S. in Ceramic Science and Engineering from Rutgers University and a M.S. in Ceramic Science and Engineering from Rutgers University. In addition, he has published various articles on thick film resistors, conductors, and component metallizations, LTCC materials, and fiber optic materials.

S3

Introduction to High Reliability Soldering for Operators and Technicians

Instructor: Joel A. Weiner, The Johns Hopkins University Applied Physics Laboratory

Enrollment limited to 12 students

Workshop Summary:

This course will focus on the requirements and techniques for the production of high reliability hand soldered connections. The overview will cover scientific, technical, and practical aspects, and include a "hot-iron" activity. A NASA-certified soldering instructor will cover the metallurgy of solders, required basic bench-level equipment, component preparation, soldering methods, storage, cleaning, electrostatic discharge damage prevention, inspection/test procedures, and criteria for acceptable soldered connections.

Techniques for assembly and soldering of a variety of component types and mounting configurations will be covered. These include soldering of terminals to boards, dual in-line packages, through-hole parts, lapped joints, high voltage components, and connectors. If they wish, students will have an opportunity to solder a variety of components to a printed wiring board.

Benefits:

- Understand the drivers and issues important to high reliability hand soldering.
- Learn what is needed at a work bench that is intended for high reliability soldering.
- Recognize acceptable and unacceptable solder connections.
- Experience the thrill of hand soldering.

Who Should Attend:

This course is intended for intermediate level soldering operators and technicians; for supervisors responsible for their performance; and for anyone wishing a better understanding of the high reliability hand soldering process.

Special Course Materials:

All attendees will be given copies of NASA-STD-8739.3, "Soldered Electrical Connections," and the "Student Workbook for Hand Soldering," NASA, December 1998, as well as course notes.

Joel Weiner has thirty years experience in printed circuit board production, microelectronic assembly, high reliability electromechanical device fabrication, inspection and quality assurance. Presently he is the Quality Assurance and Improvements Manager of the Technical Services Department at the Johns Hopkins University Applied Physics Laboratory. He is a Member of the Principal Professional Staff, and has previously been both the Assistant Group Supervisor of the Microelectronics Group and of the Electronic Services Group. Joel has a B.S. (Brooklyn College, City University of New York) and an M.S.(Rutgers University) in chemistry, and an M.S. in Technical Management (Johns Hopkins University). He has nearly forty publications, presentations and patents in related fields. He is certified by NASA as an Instructor for Hand Soldering.

International Reception
sponsored by:
Sikama International, Inc.

Exhibit Hall Aisle Signs
sponsored by:
CoorsTek

1/2 Day Course
9 AM – Noon

S4
Lead-Free Solders – Technology and Applications

Instructor:
Dr. Jennie S. Hwang, H-Technologies Group, Inc.

Course Description:

This course is to provide attendees a good understanding of lead-free solder from application perspectives, and to facilitate selection of lead-free compositions. These include technological base, product assessment, manufacturing consideration, and comparison among various lead-free compositions. Information is applicable to all types of packages and assemblies including QFP, BGA, Flip Chip and CSP.

What you will learn
- Gain an overall grasp of lead-free soldering
- Understand key parameters that are important to the selection of lead-free compositions
- Identify priority properties in a manufacturing environment
- Compare relative strengths and weakness of various systems
- Acquire knowledge and insights of future perspectives of solder interconnections
- Learn the slate of candidate alloys
- Receive objective recommendations

Topics covered
- Global legislation status – US, Japan, Europe
- New compositions vs. known binary Sn-Cu, Sn-Bi, Sn-Ag, Sn-Sb, Sn-Zn, Sn-In, systems
- Pros and cons of various lead free alloy systems
- Technology base of lead-free development
- Lead-free surface finish on PCB
- Lead-free component coating
- Differentiation of solder joint failure modes between Sn/Pb and lead-free
- Reflow profiling for lead-free soldering
- Manufacturing factors – cost vs. performance
- Selection criteria of various lead-free systems and compositions
- Strengthened characteristics of lead-free alloys
- Recommendations to manufacturers

Who Should Attend?

The workshop will benefit those who have an interest in the development of lead-free solder or in using lead-free solder for electronics packaging and assembly manufacturing. This may include researchers, manufacturing engineers, design engineers, quality assurance and materials and safety personnel. Management and decision-makers can benefit from this workshop in forming and implementing manufacturing strategies through a general understanding of lead-free solders.

Special Course Materials:

All attendees will receive a complimentary copy of the book Modern Solder Technology for Competitive Electronics Manufacturing, by Jennie Hwang, McGraw Hill, 1996 (List price $75) and a set of course notes.

1/2 Day Course
1:00 PM – 5:00 PM

S5
Solder Joint Reliability - Manufacturing Perspectives

Instructor:
Dr. Jennie S. Hwang, H-Technologies Group, Inc.

Course Description:

This course is to provide attendees a proper level of understanding of solder interconnection reliability in material basics, manufacturing know-how, and real-world performance, as well as the interrelation between them. This understanding is important to every step of manufacturing, from design and material selection, to the establishment of production process, and to the overall quality and performance of end-use packages and assemblies. Information is applicable to all types of interconnections including fine pitch QFP, BGA, Flip Chip, CSP, and passive components.

What you will learn
- Improved processes to achieve solder joint reliability
- How to avoid potential problems of solder assemblies
- Solder joint reliability factors
- Solution or recommendation to the specific problems or concerns; attendees are encouraged to bring along their production floor problems for discussion and solution. For those problems requiring a lab-examination, a complimentary preliminary assessment report will be provided to the attendee after the lecture (limit one per company)
- Future demands on solder interconnections

Topics
- What does it take to derive a universal life-prediction model
- Basic level of material fundamentals in solder alloys, alloy in response to temperature changes during service life, and solder alloy selection parameters
- Bulk solder vs. solder joint properties and the key factors that affect solder joint integrity
- Reliability factors of BGA array and QFP peripheral solder joints
- The role of gold, intermetallics, solder mask, palladium
- Basic failure process and principle in creep, fatigue, thermal fatigue
- Effects of large voids and reflow process parameters
- Microstructure vs. reflow profile vs. solder joint behavior
- Common failure modes of QFP, PBGA, CBGA, CSP and other types of solder joints
- Approaches to further strengthen solder materials in improving creep-fatigue resistance

Who Should Attend?

This course is an overview of solder joint reliability, designed to provide a working knowledge to all who are involved with or interested in surface mount/fine pitch/ BGA assembling. The course will provide new personnel to the industry with the necessary understanding of solder joint reliability issues and provide experienced personnel with insights into future technology advances.

Special Course Materials:

All attendees will receive a complimentary copy of the book BGA and Fine Pitch QFP Interconnections by Jennie Hwang, Electrochemical Publications, Great Britain, 1995 (List price $140), and a set of course notes.

Dr. Jennie S. Hwang has been a major contributor to SMT industry since the inception of SMT in PCB industry. Her primary interests are global market trends and technological development, particularly in SMT packaging and assembly. She is a highly popular lecturer/featured speaker worldwide and frequently solicited consultant to U.S. government, OEMs and SMT manufacturers.

She received her Ph.D. in Materials Science & Engineering from Case Western Reserve University and two M. S. degrees in Liquid Crystals and Chemistry from Kent State University and Columbia University. She is the author of over 150 publications, including the sole authorship of several textbooks related to electronic assembly and packaging. She writes the monthly column of SMT magazine, addressing critical industry issues. She is a member of the National Academy of Engineering and a fellow of ASM Int'l. She has received many honors and awards, including the Kent Van Horn Distinguished Alumni Award of Case Western Reserve University, U.S. Congressional Certificates of Recognition and Achievement, and The Hall of Fame—Women in Technology. Dr. Hwang serves on the Business Review Board for U.S. Government programs and on many boards and committees. She was national president of SMTA. She has over 25 years of manufacturing and business experience in the industry, having held senior managerial and research positions with Lockheed Martin, Hanson, PLC, and IEM. Dr. Hwang is currently president of H-Technologies Group, Inc. The company provides manufacturing and business solutions to the electronic packaging and assembly industry.

S6

Adhesion Science and Technology

Instructor:
Kash Mittal, Ph.D., Editor, Journal of Adhesion Science and Technology

Course Description:

Adhesion between similar or dissimilar materials is of cardinal importance in many technologies, *inter alia*, packaging. So the need to understand and control factors which affect adhesion is quite patent. Also, the durability of the bond (on exposure to process chemicals, moisture, corrosives, etc.) is of grave concern and importance.

This course will provide information on the factors affecting adhesion between different materials and how to harness the principles of adhesion in solving real problems. In this course the emphasis will be on the adhesion aspects of polymeric materials (used as coatings, adhesives, encapsulants, barriers, etc.) on a variety of substrates (metals, ceramics, plastics). The course is quite applied in nature with emphasis on concepts and principles.

Who Should Attend?

Research, development, process, production and manufacturing personnel who have a current or anticipated need for knowledge of adhesion should find this course of interest.

Dr. Kashmiri Mittal was associated with IBM Corporation from 1972 through 1993. Currently, he is teaching and consulting worldwide in the broad areas of adhesion as well as surface cleaning. He has initiated, organized and chaired a number of international symposia, and is the editor of fifty-four published books as well as others which are in the process of publication, dealing, for example, with adhesion measurement, adhesion of polymeric coatings, polymer surfaces, adhesive joints, polyimides, surface modification, and surface cleaning. He has received many awards and honors including the 1990 Dudley Award of the ASTM, the 1995 Thomas D. Callinan Award of the Electrochemical Society, the Adhesives Award, is a Robert L. Patrick Fellow of the Adhesion Society, and is listed in many biographical reference works. He is a founding editor of the Journal of Adhesion Science and Technology, and is a member of the editorial boards of a number of scientific and technical journals. Dr. Mittal was recognized for his contributions and accomplishments by the worldwide adhesion community, who organized, in his honor, the 1st International Congress on Adhesion Science and Technology in Amsterdam, 1995.

S7

Advanced Materials for Microelectronic, Optoelectronic and MEMS Packaging and Thermal Management

Instructor:
Dr. Carl Zweben, Composites Consultant

Course Description:

Materials selection impacts performance, reliability and cost. Increasingly, the traditional materials used in microelectronic packaging are failing to meet the requirements for optoelectronic and MEMS packaging, as well as those of new microelectronic system designs. In response, numerous advanced composites and monolithic materials have been, and are continuing to be developed. Property improvements include:

- extremely high thermal conductivities (over four times that of copper)
- low, tailorable coefficients of thermal expansion
- extremely high strengths and stiffnesses
- low densities
- low cost, net shape fabrication processes

Payoffs include:
- improved fiber alignment
- reduced thermal stresses and warpage
- lower junction temperatures
- simplified thermal design
- possible elimination of heat pipes
- weight savings up to 80%
- size reductions up to 65%
- increased reliability
- potential cost reductions

These materials provide the engineer with greatly expanded design options. Costs are continuing to decrease, making composites increasingly economically attractive. For example, some parts made of Al/SiC, a metal

matrix composite first used in optoelectronic and microelectronic packaging by the instructor in the 1980s, are now selling for the same price as the copper ones they replace. Use is increasing 10% annually. Newer materials offer significant advantages over Al/SiC. Advanced composites and monolithic materials will be the packaging materials of choice in the 21st century.

Advanced materials, such as Al/SiC metal matrix composites and carbon fiber-reinforced polymer matrix composites, are now being used in a growing number of high volume commercial and aerospace production applications at the rate of millions of piece parts annually. The expanding list of components includes carriers, heat spreaders, pin-fin heat sinks, solid and flow-through PCB cold plates, microwave modules, power semiconductor modules, and heat pipe overmolds. Products using these materials include cellular telephones and base stations, laptop computers, hybrid and electric vehicles, data storage drives and aircraft and spacecraft electronic systems.

This course provides an in-depth discussion of the materials, their properties, the processes by which they are made, and where they are being used. We also look at future directions in the technology.

Who Should Attend?

Engineers, scientists and managers involved in microelectronic, optoelectronic and MEMS packaging design, production and R&D. Packaging material suppliers.

Dr. Zweben, is an independent consultant on composites and technical advisor to the Georgia Institute of Technology NSF Packaging Research Center. He was for many years Advanced Technology Manager and Division Fellow at GE Astro Space, later acquired by Lockheed Martin, where he directed the Composites Center of Excellence. Previous affiliations include Du Pont and Jet Propulsion Laboratory. Dr. Zweben was the first, and one of only two winners of both the GE One-in-a-Thousand and Engineer of the Year awards. He is a Fellow of ASME, ASM and SAMPE, an Associate Fellow of AIAA, and has been a Distinguished Lecturer for AIAA and ASME. He is an internationally recognized expert in his field, with over 30 years of experience in commercial and aerospace composites technology. Dr. Zweben began working on aramid printed wiring boards (PWBs) at Du Pont in the 1970s. He continued the development of advanced composite packaging as director of the GE Aerospace Group Advanced Composites Center of Excellence, where he worked on low-expansion PWB programs and developed the first silicon carbide particle-reinforced aluminum (Al/SiC) microelectronic and optoelectronic packages. He has to his credit over 100 contributions to journals, handbooks and encyclopedias and has presented over 100 invited lectures, including one at the AIAA 50th Anniversary "Learn from the Masters" series. Dr. Zweben is Co-Editor-in-Chief of a 6-volume work, "Comprehensive Composite Materials." *He has directed and lectured at over 150 classroom, satellite broadcast and videotape short courses in the US and Europe, including courses on advanced packaging materials at IMAPS, NEPCON and Semi-Therm.*

S8

Surface Mount Technology and μBGA, CSP and DCA

Instructor:
John Kratz, NTCm Technical Director

Course Description:

These new package types will be defined and integrated into the OEM and EMS market environments by use of the Semiconductor Roadmap three and five years out. Topics of discussion will include Land Pattern development using IPC-SM-782A (amendment "A") and "non-standard" land patterns, Design for Manufacture (DfM), Materials Control and Management (MCM), industry "best practices" and Deployment Metrics for Manufacturing (DMM). This presentation will integrate the present and standard surface mount manufacturing practices with those package types that may require additional process considerations and/or modifications of accepted "best practices." These considerations will be developed with the goal of using "drop-in" or new deployment requirements while maintaining high yield and reliability metrics.

Major process steps will be reviewed which will include the following: 1) solder paste printing, 2) component pick and place, 3) solder reflow, 4) component encapsulation, 5) decontamination cleaning, 6) inspection methodology, and 7) rework techniques and issues with the goal of deploying process "additions" to existing continuous-flow manufacturing capability. Comparisons and case studies will enable the attendee to gain a quick understanding of the important issues related to new technology package types and their assembly requirements.

Who Should Attend?

This course is useful to the advanced process engineer, quality assurance, and manufacturing process engineer who requires a "knowledge-base" for expanding manufacturing capability within the framework of the package types discussed. Additionally, marketing and procurement personnel may desire to expand their knowledge of the way in which new manufacturing technology will effect their positions, capability and/or company requirements.

Special Course Materials:

The course outlines and notes will be provided to each attendee in the form of a workbook with problems and comparisons included.

John Kratz is project manager at the NATIONAL TRAINING CENTER FOR MICROELECTRONICS (NTCm) for various activities related to coordination and development of new manufacturing process requirements, selection of equipment and materials, deployment and characterization of new process and workforce training of these process requirements within a given company infrastructure. John directs research, development and writing of procurement guidelines, quality manuals and procedures for the audit of incoming and in-process functions, workmanship standards, manufacturing process instructions, and international subcontracting functional documents.

S9

Physics-of-Failure Based Application Specific Reliability Assessment of Electronic Systems

Instructor:
Patrick McCluskey, Ph.D., University of Maryland

Course Description:

For next-generation electronics, it is no longer practical to design a product for an unspecified environment, and then measure and improve the reliability of the product by

a series of test and fix steps at the latter stages of development. Fast and cost-effective product development requires that reliability be assessed for the application environment of interest in the earliest stages of conceptual design, with prototype testing used only to confirm that the designed-in level of reliability has been achieved. This reliability assessment methodology must be fast and cost-effective to permit the development of products with more features and higher quality at lower cost in a time frame commensurate with today's shorter design cycles and faster times to market. Furthermore, it must permit the rapid qualification of components making optimal use of the manufacturer's test procedures and requiring a minimum of additional testing. Finally, it must be application-specific and based on the fundamental mechanisms by which electronics fail.

This course will present such a reliability assessment approach, which is known as physics-of-failure based application specific reliability assessment. Attendees will be taught how to apply this methodology to the qualification of components and the reliability assessment of electronic systems. The course will demonstrate how to use manufacturers' test data together with failure modeling to qualify a component for use in a particular application. The course will also demonstrate the application of this virtual qualification technique to the insertion of commercial components into harsh environment applications. The use of virtual qualification for building reliability into components, modules, assemblies, and systems will also be discussed. The course will conclude with a discussion of the probabilistic nature of reliability assessment and with a demonstration of computer-aided tools for virtual qualification and application-specific reliability assessment.

Who Should Attend?

Product and process engineers who want to know how to improve product reliability and first-pass success through the up-front incorporation of design-for-reliability techniques. Quality and reliability professionals who wish to learn the latest scientific approaches for qualification, reliability assessment, and product life evaluation. Managers and technical professionals who want to learn how to reduce development costs and improve time to market while simultaneously improving product quality and reliability.

Patrick McCluskey is an Assistant Professor of Mechanical Engineering at the University of Maryland, College Park, where he is associated with the CALCE Electronic Products and Systems Center. He is the principal investigator for projects related to computer-aided reliability assessment of microelectronics, and the packaging and reliability of electronics in high power and high temperature environments. He has co-developed and taught graduate level and executive short courses on high temperature electronics, power electronics packaging, and plastic encapsulated microelectronics. He is the author or co-author of over 50 journal and proceedings articles on his research, and the co-author of two books on electronic packaging including High Temperature Electronics. *Dr. McCluskey received his Ph.D. in Materials Science and Engineering from Lehigh University in 1991, and is a member of IMAPS and IEEE CPMT.*

S10

RF/Microwave Hybrids; Principles, Materials and Processes

Instructor:
Richard Brown, Richard Brown Associates, Inc.

Course Description:

In recent years, the demands for high frequency systems and products have been growing at a rapid pace. Coupled with the continuing development of monolithic integrated circuits, MMICs are new materials and process refinement of hybrids. As a result, system and product designers are faced with the choice between hybrids and MMICs; i.e., complete system on a chip vs. hybrids with discrete devices, or more often, somewhere in-between.

This course will begin with a short, non-mathematical review of high frequency basics. Next a comparison of MMICs and hybrids is presented. The transmission line as the basic circuit component of RF and microwave hybrids will be reviewed. Hybrid "waveguide" structures will be compared as they relate to transmission line properties. The basic materials (conductors, dielectrics and substrates) and their properties will be introduced. Their effect on impedance, circuit properties and performance will be discussed. Processing technologies suitable for RF/microwave hybrids will be reviewed. Selected packaging protocols, such as vias and bonding wires, will be discussed in light of their influence on RF/microwave performance. At the completion of this course, attendees will have a better understanding of many of the critical materials and processing factors affecting high frequency circuit performance.

Who Should Attend?

This introductory course will benefit those associated with the RF and microwave arena. In particular this course will benefit those with responsibility for design and manufacturing of RF/microwave hybrids. Supervisors, engineers and technicians involved in product development, design and manufacture are encouraged to attend.

Richard Brown is a technical and engineering consultant in hybrids, with more than 30 years experience, encompassing thin and thick film, electroplating and substrate technologies. He began his career at Bell Telephone Laboratories. After joining RCA Solid State in 1968, he transferred in 1979 to the RCA Microwave Technology Center in Princeton. In 1991, Mr. Brown joined an Alcoa Electronic Packaging technology team as program manager to implement thin film on high temperature co-fired ceramic for MCMs.

He has published extensively, most recently authoring a chapter on Thin Film for Microwave Hybrids in "Handbook of Thin Film Technology," McGraw-Hill, NY, 1998, A. Elshabini-Riad, Ed. In 1995, ISHM awarded him the prestigious John A. Wagnon, Jr. Technical Achievement Award. His text, "Materials and Processes for Microwave Hybrids," was published in 1991 by ISHM, Reston, VA.

S11

Practical Methods to Design-In and Predict Surface Mount Attachment Reliability

Instructor:
Dr. Robert W. Kotlowitz, Lucent Technologies/Bell Laboratories

Course Description:

The long-term reliability of surface

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mount (SM) solder interconnections remains an important issue in advanced electronics packaging technologies. The development of high-reliability SM circuit assemblies requires an understanding of the key reliability challenges and controlling design parameters. This intensive course describes the reliability hazard for SM connections and presents practical methods for SM attachment reliability assurance. These risk-mitigation processes support the needs of the electronics packaging R&D community, by providing robust design strategies without requiring a detailed understanding of complex SM reliability issues. Major topics include:

- Reliability hazard for SM connections, driven by the component-to-substrate mismatch in coefficient of thermal expansion (CTE) and strain-induced fatigue damage.
- Solder thermo-mechanical behavior during cyclic loading, and related fatigue damage induced by stress relaxation and creep.
- Case studies of at-risk and failed SM connections. Industry examples of non-robust SM assemblies resulting from materials CTE incompatibility, insufficient lead compliance, gold-tin intermetallics, marginal solder joint quality, and aggressive mechanical loads.
- Practical lead compliance evaluation process and specialized stiffness metric for corner-most leads, corresponding to the location of the relatively high-risk SM connections.
- Effect of lead compliance on SM attachment reliability, demonstrated via fatigue life statistics from industry accelerated testing programs.
- Representative commercial high-compliance lead designs that can mitigate the SM attachment reliability hazard.
- Weibull failure probability distribution for wear-out processes, as this statistical model relates to SM attachment fatigue failure. Representative Weibull failure statistics for recognized at-risk SM packages, including TSOPs and BGAs.
- Design-for-Reliability (DFR) tool for SM attachment, covering capabilities, technical foundation, application criteria, and limitations.
- Strategies for robust SM attachment, based on the interaction of package design, assembly technology, operational thermal environment, and product service life.
- Practical applications of the DFR tool for SM ceramic discrete components, selected SM leaded packages, and BGAs.

Who Should Attend?

This course will directly benefit researchers and practicing engineers involved in SM component design, advanced electronics packaging R&D, circuit-board physical design, SM interconnection reliability, quality assurance, and SM assembly. The course is also useful to managers responsible for SM component strategy, design standards, and procurement practices guided by attachment reliability considerations.

Robert W. Kotlowitz, Ph.D., is a Distinguished Member of Technical Staff in the Wireless Networks Group at Lucent Technologies/Bell Laboratories in Whippany, New Jersey, USA. He is actively involved in SM attachment reliability in wireless telecommunication equipment, SM assembly qualification, and accelerated stress testing (AST) for product assurance. Dr. Kotlowitz is well published in SM reliability assurance, advanced packaging, and AST at major electronics packaging and reliability forums in the USA and Europe. He has been a course leader in SM attachment reliability at electronics packaging conferences and commercial training centers in the USA, Europe, and Israel. He holds a Doctorate in Engineering (Applied Mechanics) from the City University of New York, and is a long-time member of the ASME, IMAPS, and SMTA.

Monday, October 8
9:00 am - 5:00 pm

M1
Wire Bonding in Microelectronics

Instructor:
George Harman, National Institute of Standards and Technology

Course Description:

Wire bond manufacturing defects range typically from about 1000 to 100 ppm, with exceptions to >10,000 and <50 ppm. In order to achieve the lower numbers in production, one must understand all of the conditions that affect both bond yield and reliability (since they are interrelated). This course will discuss many large and small wire bonding problems, as well as subjects of specified interest to hybrid device bonding. In addition, a number of advanced topics, such as high yield and fine pitch bonding will be covered. New developments (e.g., high frequency ultrasonic bonding), are included along with a major discussion of wire bonding to multichip modules and other soft substrates.

Wire bond testing and metallurgy (covering both aluminum and gold bonds); intermetallic compounds; cleaning for yield and reliability; failures resulting from electroplating; mechanical problems in wire bonding; new bond technologies and developments; how ultrasonic bonds are formed; and the metallurgy of gold and aluminum wire. It concludes with how TAB and Flip Chip Technology compare to wire bonding.

Included in Your PDC Registration Fee:

- Lunch on the day of your course
- Refreshment breaks
- All course materials
- PDC Reception on Sunday evening *(for Attendees & Instructors only)*
- Certificate of Attendance

Who Should Attend?

Engineers in R&D, QA, QC, manufacturing, process development, and advanced technicians. It is assumed that participants have some familiarity with wire bonding and general device assembly technologies.

Special Course Materials:

All attendees will receive a complimentary copy of Wire Bonding in Microelectronics, by George Harman, McGraw Hill, NY, 1997 (List price $65), as well as course notes and explanations.

Mr. Harman is a Fellow of the National Institute of Standards and Technology (NIST), Department of Commerce. He received a BS in Physics from Virginia Polytechnic Institute & State University and a MS in Physics from the University of Maryland. Mr. Harman has published 50+ papers, two books on wire bonding, and holds four U.S. Patents. He was the 1995 President of ISHM and is a fellow of IMAPS and the IEEE. He has presented numerous talks, and has taught courses for the University of Arizona, State University of New York, IMAPS, and IEEE, to name a few.

M2

Metal Plating for Electronics

Instructor:
Michael McChesney, McChesney, Inc.

Course Description:

Electroplated finishes provide environmentally sound and cost effective contacts and coatings for most electronic components and systems. Plating also plays a role in hybrid fabrication and assembly and semiconductor bonding. This course will provide a foundation in electrolytic and electroless plating of precious metals, copper, tin and tin/lead. Also covered will be plating for corrosion protection and testing of electrodeposited coatings.

Who Should Attend?

This course is appropriate for design, process and applications engineers and technicians as well as sales personnel and those who specify, purchase or inspect plated components. Newcomers to the field or those who wish to broaden their knowledge of plating terminology, process specifications or the surface finishing processes involved in component manufacturing will find the course worthwhile.

Mike McChesney has worked in the surface finishing field for 33 years as both a production engineer and in process development and retired from the Avionics Division of Honeywell Inc. He has a BS in Chemistry and MS in Physics. He is a certified electroplater/finisher and a specialist in electronic finishing. He is an instructor for the American Electroplating and Surface Finishing Society and the College of St. Thomas. He now works as an independent consultant in the area of surface finishing.

M3

Technology of Screen Printing

Instructors:
Art Dobie, SEFAR America - MEC Division; Rudy Bacher, DuPont

Course Description:

The purpose of this course is to increase the understanding of the screen printing process thereby improving production yield and quality. The critical and integrated components for screen, such as frames, screen mesh and emulsion are presented. Presented are some of the latest advancements in the screens, the compositions and the printing process that enable screen printing to meet future circuit density requirements.

The course is applications-oriented in terms of how to optimize the screen printing process; how to specify and use screens; rheology properties that affect the print; minimizing printing defects and trouble-shooting problems related to the screens and the printing process.

Who Should Attend?

This course is intended for production and process engineers, and others interested in learning how to optimize and increase the uses of the screen printing process.

Art Dobie is Manager of Technical Service and Marketing and a member of the senior management team of SEFAR America - MEC Division in Mount Holly, NJ. He has been with MEC more than 20 years since receiving his BS in Screen Printing Technology in 1980 from California University of Pennsylvania's School of Science and Technology. Art is an original instructor of IMAPS' Technology of Screen Printing *Professional Development Course, and has delivered many technical papers and presentations relating to screen printing technology to the microelectronics industry at the local, National and International levels. He is a Senior Member of IMAPS and has held numerous offices in the Keystone Chapter, including president. Art Dobie was Co-Chair of Exhibits for ISHM '97 and initiated the IMAPS Educational Foundation Silent Auction. On October 7, 1998, Art was inducted into the Academy of Screen Printing Technology, a body of 50 technical authorities representing the highest plane of technical expertise in the screen printing industry.*

Rudy Bacher has worked 37 years in Thick Film Technology for DuPont Research and Development as a Ceramic Engineer and currently as a Development Associate. He is a recipient of the ISHM Technical Achievement Award-1984; Corporate Marketing Excellence Award-1994; and IMAPS Instructor "Technology of Screen Printing" 1990-1998.

M4

Microvias and Embedded Passives

Instructor:
Dr. Rolf Funer, Ph.D., Industry Consultant

Course Description:

New PCB designs are requiring more and more component placements, more I/Os, tighter dimensions. Microvias can dramatically reduce board size, increase I/O count and reduce layer count. The numbers of passives: resistors and capacitors are increasing dramatically. By embedding the passives directly in the circuit board, valuable surface area can be saved. And performance, particularly at high frequency, can be improved. These new technologies can work together to cut weight and size—and ultimately cost. But can these concepts be implemented today? Or are they future technologies? This workshop addresses these issues, reviews all the currently available materials and processes to make microvias and embed passives. Design and testing issues, performance, reliability, applications and economics are all covered. The design and project managers attending this course will come away with an informed view if their designs are ready for microvias and embedded passives and if microvias and embed-

ded components are ready for them. PCB manufacturing and development engineers will learn what they will need to do to implement these technologies.

Who Should Attend?

This course would be suitable for engineers who are contemplating manufacturing microvia-based circuits as well as engineers and program managers who are considering incorporating microvia circuitry into their product.

Rolf E. Funer is currently a consultant to the electronic industry. His clients include component manufacturers, electronic materials, test instrument and circuit suppliers. He recently retired from AMP Corporation as Chief Technologist, Circuits and Electronic Packaging. Previously he was Technical Director for Carolina Circuits, an AMP subsidiary. Dr. Funer spent 5 years with ICI where he was Technical Director of its Electronics Division, where the new concepts of molded circuits and high density plated ceramic circuits were developed. Earlier, Dr. Funer worked at DuPont Company for 18 years in various electronic materials research, development and marketing positions. Dr. Funer holds a Ph.D. in organic chemistry from the University of Wisconsin and a BS degree in chemistry from Loyola University.

1/2 Day Course
9 AM - Noon

M5
The Greening of Microcircuitry

Instructor:
Nihal Sinnadurai, Consultant

Course Description:

The pervasive use of electronic equipment, both consumer and industrial, has historically ignored the adverse affects of its methods, its production materials, and of the disposal of its waste. Little consideration had been given to the total impact on our lives, our health and our long-term environment.

Electronics is publicly perceived as a clean, high technology industry, solely creating benefits for mankind. The electronics industry is becoming increasingly aware of the environmental impact due to its use of heavy metals, process chemicals and cleaning fluids, all of which are considered deleterious to the atmosphere, soil and water. Predictably, there have been an increasing number of environmentally conscious government initiatives in Europe, Japan and USA to reduce the negative impact to the environment by the electronics industry.

Key areas addressed by the course include the replacement of lead-free solders, the replacement of ozone depleting cleaning agents, miniaturization (reducing the amount of hazardous materials used), energy minimization (both in manufacture and use), and product disposal.

Who Should Attend:

This course will benefit those who have the responsibility of reducing the negative impact of the electronics industry on the environment. This will include industry management, engineering, manufacturing, safety and environmental personnel.

Dr. Nihal Sinnadurai was, until recently, Principal Consultant at TWI, a world-class research and technology center for materials joining technology. Since 1982 he has been a Senior Expert of the UN Development Programme (UNDP) and the International Telecommunications Union (ITU) where he has worked to establish electronics technology, along with quality and reliability methods in developing countries. He was appointed Professor of Electronics Technology at Middlesex University in 1994 and headed its Microelectronics department from 1994-1995. Previously he was departmental manager at BT Labs where he led teams developing electronics research and development and software development for intelligent telecommunications systems. He has considerable industrial experience in electronics technologies, testing and reliability development. His inventions include the HAST non-saturating autoclave test system and liquid crystal micro-thermography. He has authored over 60 papers and contributed to 6 books within electronics. Since 1982 he has also been involved in professional development training throughout the world, and was instrumental in creating and delivering a range of intensive training programmes in electronics technology and reliability. At TWI, he developed new joining technologies and reliability methods, including a program of professional development training on microtechnology and microelectronics, which obtained IEE Institute of Physics and Institute of Materials accreditation. He holds a BSc (Honours) and MSc in Physics from the University of London, and a PhD in Reliability from the University of Southampton; he also holds fellow awards from The Institute of Physics, IEEE, and IMAPS.

M6
Fundamentals of Hybrid Microelectronics

Instructor:
Jerry Sergent, Ph.D., Consultant

Course Description:

This introductory course will cover the materials and processes used to manufacture hybrid circuits, the design process for hybrid circuits, their applications, and where the hybrid technology fits into the overall electronic packaging technology. Design, assembly methods, and applications in automotive, microwave and power telecommunications using hybrid circuits will be considered.

The materials and processes utilized to fabricate thick and thin film hybrid substrates, including thick film pastes, screen printing, firing, substrate materials, film deposition and laser trimming are covered in considerable detail. Also included are copper metallization processes, such as direct bond copper and active metal brazing.

The discussion of assembly processes includes epoxy bonding, soldering, cleaning, tape automated bonding, flip chip attachment and wire bonding. The section on packaging includes both hermetic and non-hermetic approaches. The properties of passive components utilized in hybrid microcircuits are presented.

The course concludes with a discussion of hybrid design procedures and guidelines.

Who Should Attend?

This course will be useful to those people new or peripheral to the hybrid industry. Members of electronics design groups (including management), purchasers of hybrids or electronic components, those who sell hybrid circuits or related equipment and materials, and those who are using or manufacturing hybrids also would benefit from the course content.

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Special Course Materials:

All attendees will receive a complimentary copy of the book Handbook of Hybrid Microelectronics, by Jerry Sergent and Charles Harper, McGraw-Hill, NY, 1995 (List price $90), and a set of course notes.

Dr. Jerry Sergent is a Consultant in the Electronics Packaging Industry. He is a Past President of IMAPS and a recipient of the Daniel C. Hughes Award, the William D. Ashman Award, and the John Wagnon Technical Achievement Award from this organization. Dr. Sergent has over 30 years of experience in hybrid technology and is the author of two books, "Handbook of Hybrid Microelectronics" and "Thermal Management Handbook of Electronic Assemblies." He has also published more than 70 technical papers. He was recently appointed as Editor of the IMAPS Journal.

M7

Advanced Organic Substrate Package Design & Manufacturing for RF & Broadband Applications

Instructor:
Hassan Hashemi, Rockwell Semiconductor

Course Description:

The objectives of this course are to review design and manufacturing practices and tradeoffs affecting current and next generation RF & GHz Packaging using laminate substrate technologies in single or multiple die packaging format. The course material is primarily based upon the instructor's experience on current practices used for Wireless & GHz IC packaging for Internet infrastructure applications. The course is designed for engineers or engineering managers who want to understand more about laminate single or multi chip modules, and the unique requirements for assuring that packages can be manufactured in a high volume commercial application and meet stringent electrical and thermal performance requirements.

Who Should Attend?

The course is intended for both the packaging expert (Electrical and Mechanical Engineers) as well as persons new to the field. The course will concentrate on extending the existing organic substrate infrastructure capability to GHz high volume packaging applications. The information presented will include the theoretical background with practical methods for implementing a design. These same techniques can be applied to other high frequency single or multichip designs.

Hassan Hashemi is Director of Advanced Packaging at Conexant Systems, Inc., in Newport Beach, California. He is currently managing design and development of single and multi-chip packages for broadband digital, mixed-signal, and RF devices used in personal communication applications. He holds a Masters degree in electrical engineering from the University of Texas at Austin, and has over 16 years of experience in microelectronics package design, manufacturing, and product development. Prior to joining Conexant, he was a senior member technical staff at Microelectronics and Computer Corp. and Advanced Micro Devices. He holds 10 US patents, has authored three book chapters and over 40 technical papers in the areas of high speed package electrical and thermal design and implementation.

M8

Failure Analysis of Hybrid Microelectronics Packaged Devices from a Materials Perspective

Instructor:
Andrew M. Hirt, Materials Research Laboratories, Inc.

Course Description:

In the last few years, hybrid microelectronics devices have undergone a dramatic change in the scope of materials associated with them. In the past, a hybrid device generally consisted of a ceramic substrate mounted in a metal package and contained surface mount devices on a pattern that was screen printed over the ceramic. The circuitry was generally encased in a metal package and hermetically sealed for protection. The new 'hybrid' can be a composite of almost any materials. Current substrate materials include ceramics, epoxy-glass circuit boards, flexible metallized polymers, plastics and anything else to which someone can find a way to attach a circuit pattern. Packages may be metals, ceramics, plastics, epoxies or missing altogether. With this no-holds-barred attitude toward applicable materials, the ability to perform a successful failure analysis study becomes much more difficult. Adding to the problems associated with failure analysis studies is that the hybrid has moved from primary usage in military and aeronautics applications to virtually any item that requires some form of electronic control. The local environments have expanded to the very harsh while the protection provided many hybrid circuits by encapsulation or sealing have diminished. A benefit to the overall performance of current hybrids is that the problems are generally identified, corrected and implemented quickly. A further downside, however, is that tracking the problem that caused the failure to its root source may involve several industries, shipments and plants, many of which may not have the needed records, retains, etc., that can produce useful results. In addition to the proliferation of problems associated with hybrid production, the number of analytical tools available to the failure analyst has expanded.

This short course will provide a structured approach to the failure analysis of hybrid microelectronics devices. The course will include discussion of the selection of analytical protocols and techniques and the interpretation of results. The information presented will offer insights into the root cause of failures from the materials perspective. These might include original design faults (usually assumed to have been eliminated prior to production implementation), materials failures due to processing (mechanical, chemical, etc.) or environment, shipping and handling damage, etc.

Who Should Attend?

This course will be useful to those involved in the analysis of hybrid microelectronics devices that have experienced failures, particularly for unknown reasons after prior successful manufacture. Members of electronics design groups, quality control departments and research and developments groups. Course notes will be provided.

Andrew M. Hirt was awarded a degree in Physics from the Case Institute of Technology where he had been associated with the Department of High Energy Physics and with the Thin Film Physics Laboratory. Since 1975 he has been involved in the application of surface analytical instrumen-

tation to the study of solid materials. In his involvement as founder and senior scientist with Materials Research Laboratories, Mr. Hirt has studied the surface physical and chemical characteristics of many different materials systems including numerous electronic and microelectronic products, surface cleaning/preparation processes and solid/liquid and solid/gas interactions. He has studied the surface chemistries of several metal and polymer systems extensively and has developed numerous cleaning/modification processes for various industries. Author or editor of fifty papers, presentations and books, he is a member of and has served on the executive boards of several professional societies and actively participates in local, national and international meetings and symposia. Mr. Hirt is listed in American Men and Women of Science.

M9

Critical Materials Factors in High Performance Electronics

Instructor:
Charles A. Harper, Technology Seminars, Inc.

Course Description:

This course will detail both the critical electrical and critical non-electrical parameters, which are vitally important to success in modern electronic assemblies and systems. In addition, the material presented will discuss the various substrates, especially circuit boards and ceramic substrates, and will address the new, high performance substrates. Tradeoffs for these substrates will be presented along with advantages and limitations of the high performance substrates. Other materials and material forms which are critical in today's high packaging density, high speed circuitry, and other high performance parameters will also be discussed.

For critical electrical parameters, the key electrical properties will be defined and illustrated, and the effects of major operating environments will be explored. Discussions will cover all electrical functions, including resistance and resistivity, voltage, and loss functions such as dielectric constant and dissipation factor and their variations. Often not understood anomalies of these functions will also be reviewed.

For critical non-electrical parameters, discussions and explanations will parallel those listed above for critical electrical parameters. Particular emphasis will be placed on properties of importance in the highly sensitive operational environment of thermal excursions, which almost always lead to failure problems in electrical equipment. These properties include thermal expansion, thermal stability and thermal life, and thermal conductivity. Methods for optimizing materials performance will be discussed. Other critical operating environments, and materials performance in these environments will be analyzed, along with methods for optimizing performance.

Who Should Attend?

This course will be useful for all of those interested in understanding critical materials properties and the performance and optimization of materials for important operating environments. This includes engineering, manufacturing, process, quality, marketing, and others involved in development, design and manufacture of electronic assemblies and systems.

Special Course Materials:

All attendees will receive a copy of the new Electronic Packaging and Interconnection Handbook, by Charles A. Harper, McGraw-Hill, 2000 (List price $125), and a set of course notes.

Charles A. Harper is President of Technology Seminars, Inc., of Lutherville, Maryland. He is widely recognized as a leader in materials for product design, having worked and taught extensively in this area. Mr. Harper is also Series Editor for the Materials Science and Technology Series, and the Electronic Packaging and Interconnection Series, both published by McGraw-Hill. He has been active in many professional societies, including the Society of Plastics Engineers, American Society for Materials, and the Society for the Advancement of Materials Engineering, in which he holds the honorary level of Fellow of the Society. He is a Past-president and Fellow of the International Microelectronics and Packaging Society. Mr. Harper is a graduate of the Johns Hopkins University, Baltimore, Maryland, where he has also served as Adjunct Professor.

M10

Fundamentals of Fabrication and Packaging of MEMS and Related Micro Systems

Instructor:
Ajay P. Malshe, Ph.D., University of Arkansas

Course Description:

This introductory course will cover packaging and integration of micro-electro mechanical systems (MEMS). Unlike integrated circuit (IC) packaging, MEMS packaging is highly *application specific*. MEMS and related micro systems are designed, fabricated and packaged for various applications, for example accelerometers, gyros, RF switches, optical switches, micro fluidic drug delivery systems, etc. Moreover, growing trend demands multifunctional systems where integration of these diverse signals results into true "mixed signal systems." Hence, a growing number of products need application-specific design, materials, fabrication and assembly processes for building reliable MEMS systems.

The course has two sections. The first will introduce and discuss fundamentals of various MEMS and related microsystem products, and their packaging and assembly requirements. It will further touch upon the basics of surface and bulk micro machined MEMS fabrication processes including M4 techniques and various materials used to make these devices. The second part will discuss in length classification of MEMS packaging processes, packaging and assembly issues such as dicing, stiction, interconnection, out gassing, ambient specific packaging, reliability, etc. The course concludes with a discussion of MEMS market and manufacturing trends.

Who Should Attend?

MEMS and related micro systems packaging business offers new opportunity to traditional IC packaging scientists, engineers and businesses. Further this area is evolving rapidly and hence, understanding the fundamentals is key for developing and packaging reliable products. Thus, this course is useful to scientists, engineers and business

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managers working in the areas of designing, fabrication, assembly, testing, and marketing of materials, software, equipment and processes for MEMS and related products. Also, this course will benefit people looking for new business opportunities, which are there worldwide.

Ajay P. Malshe, Ph.D. (1992), is an Associate Professor at the Department of Mechanical Engineering and an adjunct faculty with High Density Electronics Center (HiDEC), Department of Electrical Engineering, University of Arkansas, Fayetteville, AR. He is a Materials Scientist and Engineer. His two distinct fields of research interest are integration and packaging of MEMS and related micro and nano systems, and surface engineering for meso and macro systems. He has authored over eighty referred publications, holds four patents, contributed one book chapter and has delivered numerous invited talks. He has achieved many awards for technical contributions. He has ongoing collaborations with large corporations and small businesses in US and has working collaborations with various organizations overseas. He is currently an active member of International Microelectronics And Packaging Society (IMAPS) through the organization of Advanced Technology Workshops (ATW), for example in the areas of MEMS Packaging and thermal management, Chairman of Thermal Management Technical Sub-committee and National Chair of ATWs. He is also the Faculty Advisor of IMAPS's local student chapter. In addition, he is a member of ASME, ASEE, and MRS professional societies.

M11

Area Array Technology – Processes, Materials, Packages and Reliability

Instructor:
Dr. Wayne Johnson, Ph.D., Auburn University

Course Description:

The increasing number of I/Os (inputs/outputs) per semiconductor chip combined with the product driven requirements of thinner, smaller and lighter weight have led the electronics packaging and assembly industry to area array packages and assembly. The new area array package and assembly approaches are replacing the traditional perimeter approaches: quad flatpacks (QFPs) by ball grid array (BGAs), thin small outline packages (TSOPs) by chipscale packages (CSPs) and chip-on-board (COB) by flip chip on laminate (FCOL). This course will begin by examining the drivers for area array packaging, then examine the packaging options, their construction and trade-offs. Substrate design requirements will be discussed including routing, pad design and the reliability impact of design. Major assembly issues are flux selection, underfilling, if necessary, and inspection. Underfilling which is not a traditional SMT assembly process is required for FCOL and often for CSPs. The underfill process and material options will be examined. Recently, wafer applied underfill material concepts for FCOL assemblies have been discussed and this new technology concept will be explored. The course will conclude with a discussion of packaging reliability. The replacement of leads by solder spheres impacts reliability, particularly in thermal cycling and bending, and must be considered prior to implementing area array technology.

Who Should Attend?

This course is designed for staff members, technical managers, supervisors, systems designers, and manufacturing engineers in companies using or planning to use area array packages or flip chip. Materials and equipment suppliers for area array assembly will also benefit by gaining necessary background information.

Dr. Johnson is an Alumni Professor of Electrical Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). At Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and reliability for electronics assembly. He has worked in MCM design, MCM-L, -C and -D substrate technology as well as advanced SMT, wire bond and flip chip assembly techniques. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written two book chapters in the areas of silicon MCM technology and MCM assembly. He received the 1997 Auburn Alumni Engineering Council Senior Faculty Research Award for his work in electronics packaging and assembly.

Dr. Johnson was the 1991 President of the International Society for Hybrid Microelectronics (ISHM). He received the 1993 John A. Wagnon, Jr. Technical Achievement Award from ISHM, was named a Fellow of the Society in 1994 and received the Daniel C. Hughes Memorial Award in 1997. He is also a member of IEEE, SMTA, and IPC.

Dr. Johnson received B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering. He has worked in the microelectronics industry for DuPont, Eaton, and Amperex.

M12

Integrated Circuit Packaging and Assembly Technologies - Issues and Concerns

Instructor:
William J. Greig, Greig Associates Inc.

Course Description:

This course addresses how Microelectronic Packaging and Assembly are driven by the intrinsic demands of both the Integrated Circuit, and End Product requirements for "smaller, better, cheaper." It focuses on packaging trends, namely, the BGA, the CSP, the MCM, and COB and the available assembly options that include, Chip & Wire, TAB, and Flip Chip. The course also covers High Density Interconnect substrates (HDIs). The various substrate manufacturing technologies (Thick Film, Co-fired Ceramic, and Thin Film) will be reviewed and the latest developments in high density, fine line, Printed Wiring Board manufacturing discussed. Through out the course the technical issues will be emphasized and reliability concerns addressed where appropriate.

Who Should Attend?

The course provides a comprehensive overview of microelectronic packaging and assembly and is intended for individuals in any way involved with electronics manufacturing. Discussing current and future trends, it is directed towards both the experienced or inexperienced engineer and technician, and management personnel with the "need to know." It should be of particular interest to those in support activities such as procurement, quality assurance, marketing, and program office by providing a technology

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base in support of strategic planning and implementation.

Special Course Materials:

All attendees will receive a complimentary copy of the book, Hybrid Microcircuit Technology Handbook, J. Licari, L. Enlow, 2nd Edition, Noyes Publications, 1998, and a set of course notes.

William "Bill" Greig is currently an independent consultant specializing in microelectronics packaging and assembly. His previous work experiences include RCA Semiconductor, General Electric Co., Lockheed Electronics, and NASA. His areas of expertise covers semiconductor wafer processing and assembly, hybrid circuit manufacture, and printed wiring board fabrication. He is experienced in assembly technologies such as chip & wire, TAB, and flip chip. He has been granted 6 patents and has published or presented numerous papers at the various technical symposia. He has developed and presented courses at national symposia and participated in CEE programs at U. of Wisconsin, Lehigh University and Rutgers University. He is a member of SMTA and IMAPS and is currently President of the Garden State Chapter.

Come Celebrate Octoberfest!

Tuesday, October 9, 2001
4:30 pm - 6 pm

IMAPS 2001 Exhibitors will be hosting an Octoberfest. Certain exhibitors will be offering food and beverages in the style of an authentic German Octoberfest.

IMAPS will provide each attendee with a map showing which exhibitors are participating to help make your tour as easy as possible.

Mark your calendars – you won't want to miss this event!

Interested exhibitors should contact Ann Bell via email at abell@imaps.org.

M13 **FOR STUDENTS ONLY! - FREE**

Microelectronic Systems Packaging: Careers, Technologies and Markets

1/2 Day Course • 1:00 PM - 5:00 PM

Instructor:
Prof. Rao R. Tummala, Petit Chair Professor, Director NSF-PRC, GRA Scholar
Georgia Institute of Technology

Information technology involves hardware, software, applications and services. This industry has become the largest industry surpassing agriculture that lasted more than a millennium and steel that lasted more than a century. It is becoming the driving engine for science, technology, manufacturing and services paving the way for unparalleled prosperity of people and countries that participate in it. Better than 80% of all millionaires in the U.S. during the last five years have been attributed to this industry.

Microelectronics systems packaging involves all the technologies in forming electronic systems for consumer, telecom, computer, automotive, aerospace and medical industries. These technologies typically involve all the components and their interconnections to form system level boards to provide system level functions. Microelectronics packaging is the ultimate cross-disciplinary technology that involves engineers from various backgrounds. For example: electrical design typically performed by Electrical or Electronic and Computer Engineers; thermo-mechanical design by Mechanical Engineers; development of new materials that provide the required functions by Materials Engineers; fabrication of components by Chemical Engineers; electrical test by Electrical or Electronic Engineers; IC and board assembly by Mechanical or Materials Engineers; thermal management and reliability by Mechanical Engineers; and so on. Working together as a team from all these disciplines, packaging engineers design, fabricate, integrate, test, cool and assure reliability of the entire microelectronic system.

This four-hour course will present the global microelectronics market, past and future technologies that constitute this market, the educational opportunities that are available and career prospects for a lifelong career around the world in various industries.

technical program

Tuesday, October 9
Plenary Program and Awards Ceremony
8 am - 9:40 am

Continental Breakfast at 7:45 AM

Refreshments in the Exhibit Hall: 9:40 am - 10:00 am

TA1

MEMS in Aerospace and Aeronautics Applications

Session Chair: John Champion, JHU Applied Physics Lab

10:10 am - 11:50 am

The utilization of MEMS enables a reduction of mass, volume, and electrical power, offering the opportunity for numerous solutions in space applications. The requirements for reductions in mass and volume are currently seen in the movements toward nano and pico satellites. Examples of how MEMS help in accomplishing these goals are given in the session papers.

Overview on current MEMS Fabrication Techniques and Applications
Michael Gaitan, NIST

MEMS in Aerospace Applications
Robert Osiander, The Johns Hopkins University/APL

MEMS in Space Science
Rainer K. Fettig, NASA Goddard Space Flight Center/ Raytheon ITSS

Micro-Scale Avionics Thermal Management
Matthew E. Moran, NASA GSFC

TA2

Next Generation Manufacturing Technology

Session Chairs: Nicole L Cavanah, Rockwell; Terry Baum, CTS RF Integrated Modules

10:10 am - 11:25 am

This session encompasses new developments in materials and processes. Developments in materials and processes are constantly pursued to meet customer requirements of cost, reliability, and size. The papers in this session will highlight new developments in wirebonding, LTCC, and advanced materials

A New Approach to Robust Wirebonding
Kenneth J. Huth, Semiconductor Packaging Materials

Ribbon Bondability Study of Chromium-Gold and Tantalum-Tantalum Nitride-Palladium-Gold Metallization
Jianbiao Pan, Robert M. Pafchek, Frank F. Judd, Jason Baxter, Lucent Technologies

Evaluation of Advanced Materials to Satisfy Higher Reflow and Solder Joint Life Requirements on MAP BGA
Trent A. Thompson, Motorola Semiconductor Products Sector

TA3

Microfabrication

Session Chair: Jay Jayaraj, Foster-Miller

10:10 am - 11:25 am

Increases in packaging density come from and through advances in density of all types of interconnections. This session illustrates several areas in which interconnect density enable performance or application improvements.

Fabrication and Assembly of Digital Transducer-to-Bus Interface Module (TBIM) with Directly Attached MEMS Device
Namsoo P. Kim, Nelli Amirgulyan, Chung-Ping Chien, Minas H. Tanielian, Boeing Co.

Development of Organic-Micromachined Interconnects on Si Substrates at Microwave Frequencies
D. Newlin, J. Harriss, A. Pham, J. P. Lee, Clemson University

Large Suspended Bondwire High Q Solenoid-type Inductors and SrTiO3 Thin Film Capacitors for Wireless Applications
Jae Y. Park, Yun S. Eo, Kye I. Jeon, Jong U. Bu, LG Electronics Institute of Technology

TA4

HD Organic Board Technologies

Session Chair: R. Wayne Johnson, Auburn University

10:10 am - 11:50 am

Vias are a critical issue in high density laminate substrate technology. Microvias and blind vias are two approaches to achieving higher routing densities. For laminate substrates used in packages, the solder mask is an integral layer between the laminate and the molding compound. Solder mask strength and crack resistance is important for package reliability. For flip chip assembly in the package, either the die is bumped or as described in the last paper, the bump can be fabricated as part of the PWB.

Moving to Microvias in a High Reliability, Low Production Environment
John Folkerts, Anne Dietrich, Paul Falk, Binh Le, Sharon Ling, Johns Hopkins University/ APL

Accuracy Enhancement of Blind via Depth-Controlled Drilling
Christian P. Williams, Johns Hopkins University

Strength Evaluation of Microelectronics Packaging Solder Mask Materials
Maurice Othieno, Thavarajah Manickam, Patrick Variot, Ramaswamy Ranganathan, LSI Logic Corporation

High Density Wiring Substrate with Molded Polymer-Core Bumps for Flip Chip CSP
Midori Kobayashi, Yasukazu Kishimoto, Toshiba Chemical Corporation; Kazuhito Higuchi, Susumu Kimijima, Toshiba Corporation

Student Reception

Tuesday, October 9, 2001
5:30 pm - 6:30 pm

sponsored by:

DuPont Microcircuit Materials
F&K Delvotec, Inc.
Ferro EM

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TP1
Recent Development in Wafer Level Chip Scale Packages

Session Chairs: Beth Keser, Motorola Inc.; Michael Toepper, Fraunhofer IZM

2 pm - 5:25 pm

Wafer level CSP technologies are the fastest growing class of packaging technology currently in development. This rapid proliferation is being fueled by the need for package size minimization in a host of portable computing and communication products. This session addresses advancements that are being made in WLCSP process technologies which are aimed at cost effective minimal packaging with improved board level reliability.

A Polymer Reinforced WLP / Why It Has Superior Solder Joint Reliability
Deok-Hoon Kim, Peter Elenius, Scott Barrett, Flip Chip Technologies

Assembly and Reliability of a Wafer Scale CSP
Anthony Primavera, Universal Instruments; Parvez Patel, Motorola; K. Srihari, Binghamton University

Wafer Level CSP using a Screen Printing Technique
Hirokazu Ezawa, Masahiro Miyata, Masaharu Seto, Hiroshi Tazawa, Toshiba Corporation Semiconductor Company

On-Wafer Process for Stress-Free Area Array Floating Pads
Raymond A. Fillion, Robert J. Wojnarowski, Herbert Cole, Glenn Claydon, GE Corporate R&D

Indium Bump Bonding for Cryogenic Applications
Allen C. Keeney, David M. Lee, S. John Lehtonen, A. Shaun Francomacaro, Johns Hopkins University/APL

Low Cost Solder Bumping via Paste Reflow for Area Array Packages
Ning-Cheng Lee, Benlih Huang, Indium Corporation of America

A High Density Compliant Packaging Technology Development
Delin Li, Dave Light, Tessera Inc.

TP2
Wideband Materials Characterization for RF, Microwaves, and Wireless

Session Chairs: Michael Stein, Electro-Science Labs, Inc.; Peter Barnwell, Heraeus Circuit Materials Division

2 pm - 5:25 pm

The session deals with materials issues for both radio and microwave frequencies of the spectrum, with emphasis on lead-free, low-loss dielectrics, and photo patterned conductors compatible with low temperature cofired ceramic systems. RF & Microwave design and packaging engineers need vitally the acquisition of essential electrical high frequency data on various advanced electronic materials properties to serve various basic functions including interconnects. These materials data and information mainly include the complex dielectric constant, the material conductivity, and the attenuation component. The challenging design mandates additionally electronic products possessing specific desired electrical attributes, while still meeting basic thermal and mechanical essential requirements with high reliability and good yield.

High K Low Loss Dielectric Co-fireable with LTCC
Weiming Zhang, Matthias Scheikowski, Tom Hochheimer, Peter Barnwell, Heraeus Incorporated-Circuit Materials Division; Steve Dai, Motorola Labs.

Lead Free Dielectric Tape System for High Frequency Applications
Alvin Feingold, R. L. Wahlers, S. J. Stein, Electro-Science Labs, Inc.

RF Characterisation of No-Clean Solder Flux Residues
Maeve Duffy, PEI Technologies; Liam Floyd, Paul McCloskey, Sean Cian Ó Mathúna, NMRC; Karen Tellefsen, Mike Liberatore, A. Sreeram, Alpha Metals

Thick and Thin Film, High Density Packaging, Microwave, Integrated Passives
Michael R. Ehlert, Shaul Branchevsky, National Semiconductor LTCC Foundry

Photo Patterned Conductors with LTCC for Microwave and High Density Interconnect
Peter G. Barnwell, Brent Smith, Heraeus Circuit Materials Division; Michael Ehlert, National Semiconductor Corporation

High K, High Q LTCC Dielectric Material for Microwave Application
Yun-Hwi Park, J. H. Sung, D. H. Hwang, J. M. Lee, Y. K. Chung, Samsung Electro-Mechanics Co., Ltd.

High Permittivity Materials Development for LTCC
Michael T. Lanagan, Dean Anderson, Tom Shrout, Juan Nino, Hyuk-Joon Youn, Steve Perini, Clive Randall, Penn State University

TP3
Materials

Session Chairs: Herb Neuhaus, NanoPierce Technologies; Susan Bagen, Advanced Process Concepts

2 pm - 5:25 pm

Advances in materials are the key to microelectronics packaging. The papers in this session describe a number of advances in materials used in interconnect technology, and cover both board and assembly levels.

Z-axis Interconnection for 3-D High-Density Packaging
Silke Spiesshoefer, Leonard Schaper, Kaoru Maner, Errol Porter, Fred Barlow, George Bates, Mike Lucas, Bill Marsh, University of Arkansas; Michael Glover, Northrop Grumman

A Study on the Synthesis and Characterization of $AgInO_2$ Delafossite
Jane E. Clayton, Alan P. Constant, David P. Cann, Iowa State University

Characterization of $AlMgB_{14}$ Materials: An Ultra-hard Material
Theron Lewis, Alan Russell, Bruce Cook, Joel Harringa, Iowa State University

Pre-applied Flip Chip Attachment
Scott B. Charles, Michael Kropp, Robert Kinney, Steve Hackett, Robert Zenner, Bruce Li, 3M

Technology and Material for the CSP Flux-Free Underfill Resin and Process for Electrical Connection and Physical Adhesion at the Reflow Process Simultaneously
Kenji Kitamura, Naoki Kanagawa, Tomoaki Nemoto, Shoichi Fujimori, Shinji Hashimoto, Matsusita Electric Works, Ltd.

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Characterization of Ruthenia-Based Resistors Embedded in Low Temperature Co-fired Ceramic Substrates
Shen-Li Fu, Chi-Shiung His, I-Shou University

Screen-Printed Pb(Zr, Ti)$_{03}$ Thick Films for Ultrasonic Medical Imaging Applications
Marija Kosec, Janez Holc, Josef Stefan Institute; Franck Levassort, Louis Pascal Tran-Huu-Hue, Marc Lethiecq, LUSSI/GIP Ultrasons

TP4
Thermal Management
Session Chairs: Ajay P. Malshe, University of Arkansas; Tarak Railkar, Conexant
2 pm - 5:25 pm

Demands and advances in the thermal management area are highlighted in this session through various presentations by leading researchers on topics such as miniaturized heat pipes, reliability of high power optical devices, analysis and modeling.

Synthetic Jet Based Impingement Cooling Module for Electronic Cooling
Raghav Mahaligam, Nicolas Rumigny, Ari Glezer, Georgia Institute of Technology

Experimental Study of Miniature Heat Pipe with Composite Wick of Sintered/Woven Wire
Seok Hwan Moon, Ho Gyeong Yun, Gunn Hwang, Tae Goo Choy, ETRI

Thermal Control based on Miniature Heat Pipes for 3D MCM Packaging
Frederic Michard, M. Huan, C. Combes, D. Rousset, Alcatel Space Industries

Correlation of 980 nm Heat Pump Thermal Performance with Acoustic Microscopy (SAM) Results
Gabriel Takyi, C.Beesley, R.Baettig, A. Kendall, JDS Uniphase

Failure Mechanisms in High Power Optical Device Packaging: Semiconductor Laser Diodes - A Case Study
Ajay P. Malshe, Ajit R. Dhamdhere, S.N. Yedave, W.F. Schmidt, W.D. Brown, University of Arkansas (HiDEC-MEEG); John Morales, Coherent Semiconductor Group

Numerical and Experimental Simulation of Electro-Thermal Behavior of VLSI Chips
Z. J. Delalic, Jim Chen, Richard Cohen, Dennis Silage, Temple University

Set-Top Box Thermal Design with Detailed Modeling of High Power TBGA Packages
Sam Z. Zhao, Broadcom Corporation

TP5
High Density Packaging
Session Chairs: Rajen Chanchani, Sandia National Laboratories; Scott Popelar, IC Interconnect
2 pm - 5:25 pm

In this session, several advanced, high density substrate and MCM technologies will be presented. The first two papers report a new way to process organic laminate substrate and the photoimageable low temperature co-fired ceramic substrates, with fine features. A new 3D packaging technology with embedded active and passive devices will also be presented. Next, several papers also report MCM-D technology with variety of base substrate materials.

Total Pile Curing Substrate
Katsura Hayashi, Teruya Fujisaki, Masaaki Hori, Kyocera Co.

Novel Ceramic Packages and Architectures for MST Applications Made Possible with Photoimageable LTCC
Barry E. Taylor, Larry Bidwell, Angela Lawrence, DuPont i Technologies

High-Density Multi-Layer Thin-Film Packaging Technology for High-Performance ASIC Chips
Katsumi Kikuchi, Tadanori Shimoto, Hirokazu Honda, Keiichiro Kata, Koji Matsui, Sueo Morishige, NEC Corporation

A New 3-D Module using Embedded Actives and Passives
Yasuhiro Sugaya, Toshiyuki Asahi, Shingo Komatsu, Seiichi Nakatani, Matsushita Electric Industrial Co., Ltd.

A Multi-Layer Thin-Film MCM-D Modulator for VSAT Applications
Geert Carchon, P. Van Loock, K. Vaesen, S. Brebels, W. De Raedt, B. Nauwelaers, E. Beyne, IMEC-MCP/HDIP

The PSGA, A Lead-Free CSP for High Performance & High Reliable Packaging
Bart Vandevelde, Eric Beyne, Arun Chandreshekar, Evelien Driessens, Marcel Heerman, Jef Van Puymbroeck, IMEC

The Challenge of Overcoming Wire Sweep in Ultra-Fine-Pitch Wirebonded Ball Grid Array Packages
Robert Radke, Fuaida Harun, Ruzaini Ibrahim, Lois Yong, Tu-Anh Tran, Motorola Semiconductor Products Sector

Special Session*
2:00 PM – 3:20 PM

TP6
National Science Foundation and IMAPS Educational Foundation
Session Chair: Rao Tummala, Georgia Institute of Technology

Microwave Characterization of Low Temperature Cofire Ceramics with Embedded Fluid Channels
Orfirio Sanchez, Florida International University

Electrically Conductive Adhesives Technology
James E. Morris, TJ Watson School of Engineering & Applied Science

Efficient and Economical Laser Processing of Mixed Signal Packaging
T. Darren Brown, University of Kentucky

Mechanisms of the Adhesion of Aromatic Thermosetting Copolyesters (ATSPs)/SiO_2 and ATSPs/Polyimides
Amir Alam, University of Illinois at Urbana –Champaign

*Authors are NSF/IMAPS 2000 - 2001 Award Recipients

**Presentations will be 20 minutes each.*

IMAPS Annual Business Meeting
Tuesday, October 9, 2001
11:30 AM – Noon
Baltimore Convention Center

Change of Officers

Presidents' Messages to the Membership

Annual Business Meeting

No lunch will be provided at this meeting

WA1

High Density Packaging for Portable Terminal Equipment in Japan *(Japanese Translated Session)*

Session Chairs: Yuzo Shimada, NEC Corporation; Charles E. Bauer, TechLead Corporation

8 am - 10:55 am

The leaders in mobile electronics product and technology for more than 40 years, Japan now leads again in the application of flip chip packaging techniques for today's portable consumer products. This session presents current deployment alternatives for flip chip in Japanese products and demonstrates cost effective flip chip use in telecommunication appliances, personal computing devices and other mobile products.

High Density Packaging Using Flip Chip Technology in Mobile Communication Equipment
Kazuto Nishida, Matsushita Electric Industrial Co., Ltd.

Assembly Technology for Miniaturizing of Advanced Cellular Phone
Tadao Otani, Toshiba Corporation

LTCC Module Using Flip Chip Technology for Mobile Apparatus
Jitsuho Hirota, Murata Manufacturing Co., Ltd.

The Technology of Flip Chip Bonding on Organic Substrate for PDA
Akira Makabe, Seiko Epson Corporation

Packaging Technology for Mobile PCs
Shunichi Kikuchi, Fujitsu Limited

Sn-Zn Lead-free Solder Applied Notebook Personal Computer
Motoji Suzuki, NEC Corporation

WA2

Integrated Passives in LTCC for RF, Microwaves and Wireless

Session Chairs: John Gipprich, Northrop-Grumman; Fred Barlow, University of Arkansas

8 am - 11:20 am

The session deals with integrated passives in low temperature cofired ceramic systems. Thermal management is a crucial issue to be addressed in the LTCC manufacturing process, as a potential emerging technology for telecommunications, including instrumentation, military, space, satellite communications, adaptive antennas, data and wireless transmission, directions finder, radar, electronic counter measures, threshold detection, local area networks, cellular & personal communications services (PCS), GPS, ISM, and wireless market driven products in general. Components and break through trends in passives integration, advanced devices, and elaborate systems evolve as the drive mandates higher circuit densities and realization of finer pitch patterns (reducing device junction temperature and improving the thermal resistance of the various interfaces of the planar electronic materials).

Parameterized Libraries of Embedded Inductors and Capacitors in LTCC
R. Ramprasad, Feng Ling, William Blood, Thomas Myers, Michael Petras, Aykut Dengi, Mel Miller, Motorola, Inc.

A Packaged Miniature Antenna for Wireless Networking
Bedri A. Cetiner, Luis Jofre, Franco de Flaviis, University of California

Efficient Band Pass Filter Design for a 25 GHz LTCC Multichip Module using Hybrid Optimization
Winfried Simon, Reinhard Kulke, Andreas Lauer, Matthias Rittweger, Peter Waldow, Ingo Wolff, IMST GmbH

Power Distribution Networks in Multilayer LTCC for Microwave Applications
Reinhard Kulke, Winfried Simon, Gregor Moellenbeck, Juergen Kassner, Peter Uhlig, Peter Waldow, IMST GmbH

Manufacturing of Multilayer Dielectric Ceramic Chip Antenna for Bluetooth by Using LTCC Technology
Hyun Hak Kim, Jong Yeon Lee, Tae Seok Park, Jong Myung Woo, Samsung Electro-Mechanics Company

Effect of Design and Processing Parameters on Buried Resistors in LTCC Systems
Aicha Elshabini, V. Rajagopalan, F. Barlow, W. Gangqiang, S. Ang, A. Elshabini, University of Arkansas

Glass-Ceramic Module for 60GHz-Band Wireless Communication Systems
Kazuhiro Ikuina, Takeya Hashiguchi, Masaharu Itoh, Kenichi Maruhashi, Keiichi Ohata, NEC Corporation

WA3

Advanced Wirebond

Session Chairs: Lee Levine, Agere Systems; William Greig, Greig Associates

8 am - 10:55 am

This session will expand our understanding of wire bonding process mechanisms. Although wire bonding is the most common form of IC interconnection, the welding mechanisms have not been fuly explained. The papers in this session describe DOEs using in situ sensors and advanced ultrasonic systems that expand our understanding of wire bonding and provide process capability improvements.

In-Situ Ultrasonic Stress Microsensor for Second Bond Characterization
Juergen Schwizer, Oliver Brand, Henry Baltes, ETH Zurich; Michael Mayer, ESEC Cham

Wire Bond Temperature Sensor
Shivesh K. Suman, Yogendra Joshi, University of Maryland; Michael Gaitan, George Harman, NIST

High Frequency Wirebonding: Its Impact on Bonding Machine Parameters and MCM Substrate Bondability
Harry K. Charles, Jr., S. John Lehtonen, Katherine J. Mach, Jean S. DeBoy, Richard L. Edwards, The Johns Hopkins University/APL

The Influence of Surface Defect Size on the Wire Bond Pull Strength for Automotive Lead Frame Materials
Philip W. Lees, David W. M. Williams, Barry Njoes, Eric Dextradeur, Technical Materials, Inc.

Fine Pitch 2nd Bond Evaluation for PBGA Packages: Process Capability and Reliability Assessments
Tu Anh Tran, Greg Ridsdale, Lois Yong, Burt Carpenter, Dennis Ravenscraft, Fuaida Harun, Motorola

Wire Loop Development for Advanced PBGA Packages with Multiple Rows of Bonding Fingers and Power-Ground Rings
William K. Shu, Philips Semiconductor

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WA4

Power Packaging

Session Chairs: Doug Hopkins, State University of New York; Dave Kellerman, Material Solutions® Corporation

8 am - 10:55 am

Higher power density packaging is being addressed on several technological levels. Materials and processes are being developed and applied in high power density packaging including Cubic Boron Nitride, a novel LTCC/silver metal structure, a new thermally conductive die attach material, and diamond/diamond like film materials. The papers present structures to promote power in RF, MCM and discrete MOSFETS.

High Thermal Conductivity Cubic Boron Nitride Thick Films
Peter J. Gielisse, Halina Niculescu, Jason P. Tremblay, Selim Achmatowicz, Malgorzata Jakubowska, Elzbieta Zwierkowska, Leszek J.Golonka, Tomasz Zawada, Viktor B. Shipilo, Elena Shishonok, Ludmila M. Gameza, Florida State University

Thick Silver Tape in Low Temperature Cofired Ceramic (LTCC) for Thermal Management
W. Kinzy Jones, Peng Wang, Yanqing Liu, Florida International University

Silicon Carbide Power Die Packaging in Diamond Substrate Multichip Power Module Applications
Alex Lostetter, K. J. Olejniczak, A. P. Malshe, W. D. Brown, Aicha Elshabini, University of Arkansas

Evaluation of Embedded Power Technology for IPEM Packaging Applications
Zhenxian Liang, Fred C. Lee, J. D. Van Wyk, G-Q. Lu, Virginia Tech

Hybrid Modules as an Alternative to Paralleled Discrete Devices
Don Morozowich, Robin Farruggia, Powerex, Inc.

High Efficiency Microwave Power Amplifier: From the Lab to Industry
William H. Sims, NASA - Marshal Space Flight Center

WP1

Reliability of Novel CSP Structures

Session Chairs: Ernie Vasvary, Micro Systems Engineering Inc.; James Cook, Promex

2 pm - 5:25 pm

CSP technologies are key drivers to the industry's continuing need for form factor reduction and/or improved functional integration. These technologies must also be able to withstand the stresses that hand held products are often subjected to. This session will address a range of topics related to mechanical modeling or reliability testing of CSPs at the component and board level.

Strength Characterization and Fracture Surface Analysis of Silicon Dies
Jenq-Dah Wu, S. H. Ho, Sarah Liao, P. J. Zheng, Henry Iksan, Advanced Semiconductor Engineering, Inc

Reliability Design and Experimental Work for Mirror Image CSP Assembly
Dongji Xie, Sammy Yi, Kazu Nakajima, Flextronics International

Reliability and Failure Mechanisms of Chip Scale Package on Laminate Technology
Zsolt Illyefalvi-Vitez, Pál Németh, Péter Bojta, Technical University of Budapest

FEM Analysis of Solder Pad Warpage in Elastomer Attaching Process
Jong-Kul Lee, Byoung Un Kang, Hyuk-Soo Moon, Tae-Sung Kim, LG Cable Ltd., Microelectronic Materials T/G

Reliability Evaluation of CSP Electronic Devices Package
Hideo Koguchi, Chie Sasaki, Kazuto Nishida, Nagaoka University of Technology

The Effect of Compound Properties to Three Dimension Packages
Caesar Lin, Y. P. Wang, T. D. Her, Siliconware Precision Industries Co., Ltd.

Design and Reliability Study of Wire-Bonded µBGA® Packages for DDR-DRAM Applications
Ilyas Mohammed, Sridhar Krishnan, Young-Gon Kim, Tessera, Inc.

WP2

Integrated Passive Technology with PWB & Thin Film Processing for RF and High Speed Applications

Session Chairs: Robert Heistand, AVX; Timothy Lenihan, Sheldahl

2 pm - 5:25 pm

Integrated passive technology is being driven by the RF/wireless and high speed signal integrity applications. This session focuses on technology being developed in the printed wiring board and thin film fabrication arenas. Common themes are the innovations to increase specific capacitance, or raise the Q of inductor elements available for integration. Papers are selected from academia, material suppliers and systems houses.

Thin Film Capacitors Embedded into High Density Printed Circuit Boards
Angus I. Kingon, J-P Maria, TY Kim, North Carolina State University; R. Crosswell, Motorola

Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards
William Borland, John J. Felten, DuPont Electronic Materials

Lead-free High K Dielectrics for Integral Capacitor using MOCVD
Tatsuo Ogawa, Ahmet Erbil, Swapan K. Bhattacharya, Georgia Institute of Technology

The Effect of Miniaturization of Embedded Resistors in High Density Substrates
Daniel Brandler, Ohmega Technologies, Inc.

The Integration of RF Passives using Thin Film Technology on High-Ohmic Si in Combination with Thick Film Interconnect
Joost Van Beek, Marc van Delden, Andre Jansman, Arjen Boogaard, Nick Pulsford, Arnold den Dekker, Philips Research

RF Integrated Passives in Three Dimensions
Theo G.S.M. Rijks, J.T.M. van Beek, A.B.M. Jansman, M.K. Kammerer, Philips Research

High-Value, Low-Loss MOS Capacitors for RF Decoupling
Fred Roozeboom, R. Elfrink, T. Rijks, J. Verhoeven, A. Kemmeren, J. van den Meerakker, Philips Research

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WP3

Cu Wirebond and Reliability

Session Chairs: Michael Sheaffer, K&S Packaging Materials Group; Roupen Keusseyan, Dupont

2 pm - 5:25 pm

Copper metallization (bond pads) and low K dielectrics represent the next challenge facing IC manufacturing. Advanced wire bonding techniques are required for interconnection. This session will address interconnection issues for copper metallized integrated circuits. Wire bond reliability in highly stressed and corrosive environments will also be addressed.

Wire Bonding to Advanced Copper-Low-K Integrated Circuits, the Metal/Dielectric Stacks and Materials Considerations
George G. Harman, Christian E. Johnson, NIST

Research on Prevention of Corrosion at Au-Al Bonds
Yasuhide Ohno, Takuo Shoji, Keishi Miyamoto, Isao Shimizu, Kumamoto University

Reliability of Aluminum Wirebonds in Plastic Encapsulated Packages
Pankaj Mithal, Delphi Delco Electronics

Wirebonds for Munitions Applications: Effects of Dynamic Shock, Vibration, and Spin
S. John Lehtonen, H. K. Charles, Jr., Johns Hopkins University/APL; G. Katulka, Peter Muller, N. Hundley, M. Ridgley, ARL

Back-end Assembly Solution to Bare Copper Bond Pad Wafers
Chuchung Lee, Susan Downey, Peter Harper, Bill Williams, Fuaida Harun, C. C. Yong, Motorola

A Reliable Copper Wire Bond Interface for Microelectronic Packaging
Nicole Cavanah, Rockwell International

Differences Between Aluminum and Copper Wafer Metallization in the Wafer Saw Process for Thin BGA Packages
Mark Gerber, Noel Arguello, Daniel Cavasin, Motorola-SPS

Lunch in the Exhibit Hall

Tuesday & Wednesday
October 9th & 10th
Noon - 2 PM

WP4

Lead-Free Solders

Session Chairs: R. Wayne Johnson, Auburn University; Herb Neuhaus, NanoPierce Technologies

2 pm - 5:25 pm

The electronics industry is moving to lead free assembly for environmental and market driven reasons. Solder alloys, fluxes, processing equipment, mechanical properties, and reliability are all issues that must be addressed prior to the switch to lead-free assembly. It is a very complex undertaking and this session will examine some of the key points.

Effects of Cu or Bi Additions to the Creep Properties of Sn-3.5Ag Solder Alloy Joints
S. W. Shin, D. K. Joo, Y. S. Lee, Jin Yu, Korea Advanced Institute of Science and Technology

Best Composition for Sn-Ag-Cu Lead-Free Solder
Katsuaki Suganuma, G. Kim, S. H. Huh, Osaka University

Solder Paste with Polymerizing Flux for Lead-Free Alloy Solder
Tsutomu Nishina, Kenji Okamoto, Fuji Electric Corporate Research and Development, Ltd.

Improvement of Wave Soldering Equipment for Lead-Free Solder
Shigeo Nomura, Makoto Miyazaki, Kenichi Oki, Toshiyasu Takei, Akio Yoshida, Shigeyuki Ogata, Oki Electronics Industry Co., Ltd.

Soldering Property of BGA using Sn-Bi System Solder Balls
Toshiya Akamatsu, Kazuyuki Imamura, Fujitsu Laboratories Ltd.

Thermal and Mechanical Cycling Fatigue of PBGA Assemblies with Lead-Free Solder Pastes
Krishna Jonnalagadda, Tao Bai, Bill Olson, Motorola Labs (ATC)

Ultra Low Alpha Emission Lead Free Solder for Flip Chip Bumps
Yasushi Moriwaka, Satoru Takahashi, Masayoshi Kohinata, Naoki Uchiyama, Mitsubishi Materials Corporation

Interactive Forum (Poster Session)
1 pm - 4 pm

Compact Folded-Line RF Power Dividers
Chi-Young Lim, R. S. Settaluri, V. K. Tripathi, A. Weisshaar, Oregon State University

85°C/85%RH or 40°C/95%RH? Contradictory Results in Climatic Reliability Tests
Gabor Harsanyi, Budapest University of Technology and Economics - Hungary

Alternative Underfill Material for CSP Packages: Low Outgassing and Ionics Epoxy
Michael Ko, 3M; Chin Teong Ong, 3M - Singapore

Modeling of Effects of Geometry and Temperature Cycle on Viscoplastic Deformation and Durability of FCOC Solder Joints
Qian Zhang, Yogendra Joshi, Abhijit Dasgupta, Rathindra Pal, University of Maryland

Zero Shrink Process for Cost Sensitive High Volume LTCC Applications
Mike F. Barker, Rick Draudt, DuPont Microcircuit Materials

Inexpensive Processes for Flip Chip Manufacturing
Karel Malysz, Ivan Szendiuch, Technical University of Brno - Czech Republic

Development of a Low Volume Flexible Flip Chip Process
Alan P. Boone, Rockwell International

A New Thermally Conductive Die Attach Film with Low Stress and Excellent Reliability as a Replacement for Lead Solders
Takashi Masuko, Hiroki Hayashi, Shinji Takeda, Junko Morikawa, Toshimasa Hashimoto, Hitachi Chemical Co., Ltd.

Reliability of Bumpless TAB Component: CSPs and Bare Dies, for Harsh Environment Applications
Daniel Lambert, Danielle Roze, Patrick Courant, Bull TPAM

A Study of the Effect of Fabrication Parameter Variation on Thick Film Strain Gauge Characteristics
Yulan Zheng, John Atkinson, Russ Sion, Gary Zhang, University of Southampton

Poster Papers continued......

OptoBGA™ for 10Gbps Data Link
Masahiro Kijima, Mitsuo Yanagisawa, Kyocera Corporation

Radiation Tolerant Computer for Space Environment
Anthony S. Lai, Steve Motter, Brian Dietz, Aitech Space Systems Inc.

New Direct-Write Technology for Pad Redistribution on Individual Die
Michael T. Duignan, Scott A. Mathews, David N. Wells, Daniel Anthony, Potomac Photonics, Inc.

Power Cycling and Structural Integrity Approach to Assessing Reliability of Electronic Packaging
Bor Zen Hong, Tsorng-Dih Yuan, IBM Microelectronics Division

The New Microelectronic Ignition Circuits for Sodium and Metal Halide Lamps
Janusz J. Gondek, M. Ciez, J. Kocol, W. Zaraska, Private Institute of Electronic Engineering

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IMAPS ATW on Optoelectronics

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October 11-14, 2001
Radisson Hotel Bethlehem
Bethlehem, PA

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THA1
Flip Chip
Session Chairs: Andrew Strandjord, IC Interconnect; Philip Garrou, Dow Chemical
8 am - 11:20 am

This session will be led by a survey of new flip chip applications and markets. New flip chip bumping technologies, lead-free solder alternatives, very fine pitch solder bumps and indium solders will also be discussed in this session.

Flip Chip Market Trends
E. Jan Vardaman, Linda Matthew, TechSearch International, Inc.

Lead-Free Solder Alloys for Flip Chip Applications Using Stencil Printing
Scott Popelar, Andrew Strandjord, Larry Heitz, IC Interconnect

Lead-Free Solder Bump Technologies for Flip-Chip Packaging Applications
Zaheed S. Karim, Rob Schetty, Advanced Interconnect Techonology Ltd.

Low Cost Flip Chip on Paper Assembly Utilizing Non-Thermal Cure Materials
Jad Rasul, Jan Danvir, Noel Eberhardt, Ali Tootoonchi, Motorola Inc.

Study of Underfill Resin Properties for High Performance Flip-Chip BGA Package
Yuko Sawada, Kozo Harada, Hirofumi Fujioka, Mitsubishi Electric Corporation

Novel Alignment Technologies for Wafer Level Packaging
Friedrich P. Lindner, Christian Schaefer, Bob Michaels, Thomas Glinsner, EV Group

Flip Chip Joining of Thin Chips on Flexible PEN Substrates
Erja Jokinen, Eero Ristolainen, Tampere University of Technology

IMAPS 2001 PROCEEDINGS

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THA2
Modeling & CAD
Session Chairs: Luu Nguyen, National Semiconductor Corp.; R. Panneer Selvam, University of Arkansas
8 am - 11:20 am

This session will address novel ways of modeling self and mutual frequency impedances of multiconductors in lossy substrates, equivalent circuit simulations of decoupling capacitors, thermomechanical warpage of packages with response surface methodology, CAD software for flip chip redistribution, characterization data on low loss PCB materials, thermal models for MEMS structures, and ultrawide bandwidth power devices modeling.

Improved Thermomechanical Warpage Prediction of Microelectronic Packages Using Response Surface Methodology
Eric Egan, Gerard Kelly, Tom O'Donovan, Peter Kennedy, NMRC

Controlling Capacitor Parasitics for High Frequency Decoupling
Andrew Ritter, George Korony, Carlos Gonzalez-Titman, Joseph Hock, John Galvagni, Robert Heistant, II, AVX Corp.

CAD Design for Area Pad Transformation
Yu-Jung Huang, Ching-Mai Ko, Shen-Li Fu, I-SHOU University

Computer Modeling to Optimize the Heat Removal Capacity of the Micro-Jet Array
R. Panneer Selvam, Joseph Khater, Yangki Jung, S. Ang, A. Elshabini, University of Arkansas

The HP 85192B EEFet3 GaAs FET Nonlinear Model used in the High Efficiency Microwave Power Amplifier (HEMPA)
William H. Sims, NASA - Marshal Space Flight Center

Analytic Model for Self and Mutual Frequency-Dependent Impedances of Multiconductor Interconnects on Lossy Silicon Substrates
Hasan Ymeri, Bart Nauwelaers, Karen Maex, David De Roest, Michele Stucchi, Katholieke Universiteit Leuven

Electrical Evaluation of Differential Striplines for High-Speed Backplane using TRD/TDT Measurements
Youngmin Lee, Keith Guinn, Kavita Goverdhanam, Agere Systems

THA3
Photonics
Session Chairs: Michael Wernle, NanoPierce Technologies; Phillip Zulueta, Jet Propulsion Laboratory NASA
8 am - 11:20 am

The struggle for an economic solution to greater bandwidth, lower power, lower carrier loss and lower noise over long distances has propelled Photonics and Optoelectronics to the forefront of the telecommunications industry. However, the electronics packaging of photonic/optoelectronic devices has not occurred easily for larger volume applications. This session focuses on the design, material, fabrication and assembly issues associated with photonics/optoelectronics packaging and will also highlight selected applications of this rapidly growing technology.

Design for Reliability of MEMS / MOEMS for Lightwave Telecommunications
Susanne Arney, Lucent Technologies Bell Labs

A New Methodology for Comprehensive MEMS Packaging for Opto-Electronic Applications
Roupen L. Keusseyan, D. Amey, M. Doyle, S. Horowitz, J. Sosnowski, DuPont Microcircuit Materials

Angular Alignment Considerations in Laser Diode to Microlensed Optical Fiber for Automated Photonics Packaging
Zirong Tang, Frank G. Shi, University of California, Irvine

Electrical and Thermal Performance of a New Process for High Density LED Array Assembly
Michael E. Wernle, Michael Kober, NanoPierce Card Technologies GmbH

Assembly Considerations & Critical Processes for Optoelectronic Device Assembly
Bruce W. Hueners, Palomar Technologies, Inc.

Stud Bump Flip Chip Assembly of MEMS and MOEMS
George A. Riley, FlipChips Dot Com

Optical Leak Testing of Hermetic Packages
John W. Newman, NorCom Systems, Inc.

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THA4
Advanced Thick Film Materials Technologies
Session Chairs: Harry Kellzi, Teledyne Electronic Technologies; Mike Ehlert, National Semiconductor LTCC Foundry
8 am - 11:20 am

This round up of current topics features several papers on emerging methods of fine line patterning on ceramic and organic substrates and several other current issues. These include new paste systems for high thermal conductivity Aluminum Nitride substrates, an analysis of failure mechanisms in conductors on ceramic and a method of creating low impedance thin film decoupling caps for high-speed digital circuits.

A New Paste System for AIN
Christel Kretzschmar, P. Otschik, H. GrieBmann, Fraunhofer Institute for Ceramic Technologies and Sintering Materials

Thick Film Fine Line Patterning - A Definitive Discussion of the Alternatives
Meg Tredinnick, David Malanga, Peter Barnwell, Heraeus Incorporated-Circuit Materials Division

Direct Gravure Printing (DGP) Method for Printing Fine Line Electrical Circuits
Juha Hagberg, Marko Pudas, Seppo Leppavuori, Microelectronics Laboratory and EMPART Research Group of Infotech Oulu

Sub-400C, Direct Write-able Dielectrics and Conductors for Polyimide and Other Low-T Substrates
Paul G. Clem, Nelson S. Bell, Geoff L. Brennecka, Duane B. Dimos, Sandia National Laboratiories

Fine Line Technology for BGA-Applications on Silicone Polymer Substrates
Gernot Bischoff, Gert Winkler, Technical Univ. of Ilmenau; Hubert Landeck KEW Konzeptentwicklung GmbH

The Mechanism of Thick Film Conductor Fracture on Printed Multilayer Ceramic and LTCC Substrates
Jiming Zhou, Stephen Tsai, Christine Coapman, Delphi Delco Electronics Systems

Low Impedance Thin Film Decoupling Capacitor for High Speed Digital Circuits
Shigeo Konushi, S. Nagakari, J. Takafuji, F. Fukumaru, S. Nambu, Kyocera Corporation

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Tuesday: 9:40 am - 10:00 am
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Tuesday - Wednesday: 3:15 pm - 3:45 pm

All breaks will be in the Exhibit Hall

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additonal events

Register for these events on page 32

Microelectronics Marketing Research Council (MMRC)

Fall Meeting

Optoelectronics Packaging:
Issues, Enabling Technology, and Government Policy Considerations
Westin Fairfax Hotel
Washington, DC
October 5-7, 2001

Co-sponsored by:
IMAPS & MMRC

Program Chair: E. Jan Vardaman, TechSearch International Inc.

This MMRC meeting will focus on optoelectronics packaging. Presentations focus on the market for this exciting technology, including drivers for the growth of the optoelectronics industry. Key roadmaps from around the globe are presented. Issues such as requirements for low-cost packaging solutions, material and substrate needs, assembly equipment automation requirements enabling the mass production of low-cost packages are addressed. Key U.S. Government funding activities and policies to promote the development of the optoelectronics industry are addressed by a group of distinguished presenters. Bus service provided to Baltimore, see page 32.

Registration is extremely limited! Register now!

IMAPS Advanced Technology Workshop on Optoelectronics

Radisson Hotel Bethlehem
Bethlehem, PA
October 11-14, 2001

General Chair: Tom Green, *tgreen@northampton.edu*
NTCµ, Northampton Community College

Technical Chair: Bill Heffner, *wheffner@agere.com*
Agere Systems (*formerly Lucent Optoelectronics*)

An optoelectronics packaging ATW is planned for October 11-14 in historic Bethlehem, Pennsylvania, located about 2.5 hours north of the BWI airport. The optoelectronics component industry has enjoyed a period of unprecedented growth spurred on by the insatiable desire for higher data rate transmission and increased bandwidth. This ATW will bring together scientists and engineers from industry, academia and government to address the unique technical challenges faced by all in the optoelectronic packaging arena. The workshop follows on the heels of the IMAPS National show with a Thursday night kick off and Keynote address by John Pittman of Agere Systems. Friday's session addresses the packaging challenges posed by the various device types, e.g., detectors, modulators, amplifiers, MEMS, etc., along with their associated packaging processes. Saturday's sessions are all about alignment and automation issues. The evening session will be held across the river on the scenic campus of Lehigh University, where the focus will redirect to attachment and materials issues in opto packages. Sunday morning will include a buffet breakfast and a final wrap-up session. One of the ATW's highlights will be "The new kids in town." With a multitude of start-ups in the area we'll have the chance to interact and learn first hand some of the unique packaging issues and challenges facing new start-up companies.

Plenty of social time is planned to facilitate informal interaction among attendees. You'll have the chance to develop personal acquaintances as together we exchange views and share ideas on common problems. It's a historic event you don't want to miss! Bus service provided to and from Bethlehem, PA, see page 32.

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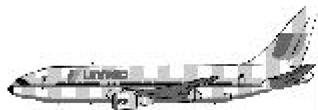

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Attendee Profile

What is your primary job function? *(please check only one)*

❑ 1. Circuit, package, module, board, or system design (including management)
❑ 2. Research and development (including management)
❑ 3. Process, manufacturing or production engineering (including management)
❑ 4. Test and measurement engineering (including management)
❑ 5. Quality Control, product assurance, or reliability assessment (including management)
❑ 6. Purchasing (including management)
❑ 7. Sales and marketing (including management)
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❑ 9. Consultant
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❑ 11. Technician or operator
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Your employer's Industry (include manufacturing and sales)
(please check only one)

❑ 1. Optical telecommunications components (photonics, electro-optics, fiber)
❑ 2. Optical telecommunications systems (photonics, electro-optics, fiber)
❑ 3. Aerospace, Avionics
❑ 4. Commercial/Industrial
❑ 5. Consumer
❑ 6. Semiconductor
❑ 7. Computing (hardware or software)
❑ 8. Communications (equipment or devices)
❑ 9. Automotive
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❑ 11. Government or military
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❑ 13. University/Education

Total Fees and Deposits

#1 Symposium Registration Subtotal *(from page 32)* $________

#2 Foundation Contribution Subtotal *(from page 32)* $________

#3 PDC Registration Subtotal *(from page 32)* $________

#4 Additional Purchases Subtotal *(from page 32)* $________

TOTAL AMOUNT DUE $__________

❑ Enclosed check payable to IMAPS $ ____________

❑ Charge My Fees to: ❑ Visa ❑ MasterCard ❑ Discover ❑ American Express ❑ Diners Club

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Cancellations will be refunded (less a $50 processing fee) only if written notice is postmarked on or before **September 21, 2001**.

No refunds will be issued after that date.

Full Symposium Registration

✓	Type (check one)	Includes	Advance on/before 9/4	On-site After 9/4
	IMAPS Member*	WR, EL, TS, EX, PR	$595	$695
	Non-member*	WR, EL, TS, EX, PR	$670	$770
	Presenters/Speakers*	WR, EL, TS, EX, PR	$495	$595
	Session Chair/Co-chair*	WR, EL, TS, EX, PR	$495	$595
	Student Member*	WR, EL, TS, EX, PR	$10	$20
	Student Non-member*	WR, EL, TS, EX, PR	$15	$25
	Exhibits Admission	WR, EX	$10	$20
	*Includes one-year membership or membership renewal at no additional charge			
		Additional Events		
	Spouse/Guest Tours	WR, EX		
	❍ Tuesday only		$90	$120
	❍ Wednesday only		$120	$175
	❍ 2-Day Package		$190	$220
	Golf Tournament		$125	$150
	Plenary Session w/Continental Breakfast...7:45 AM			**FREE**
		MMRC Fall Meeting*		
	IMAPS Member Company		$650	$750
	2nd Attendee from Same Company		$550	$650
	Non-member Company*		$1150	$1250
	*Includes one-year Organizational membership in IMAPS			
	Spouse/Guest Meals		$400	$400
❍	Bus service to Baltimore on Sunday, October 7, 2001. Bus leaves Westin Fairfax at 12:30 pm			**FREE**
	*Limited Registration for this event. Check availability after September 4, 2001			
		Optoelectronics Workshop - 4 days		
	IMAPS Member		$625	$725
	Non-member*		$700	$800
	Session Chair/Speaker		$400	$500
	Spouse/Guest Meals		$400	$400
	*Includes one-year membership in IMAPS			
❍	Bus service to Bethlehem departs from the Hyatt at 12:30 pm *(check if needed)*			**FREE**
❍	Bus service to Baltimore Washington International Airport on Sunday, October 14, 2001 departs Bethlehem at 1:00 pm *(check if needed)*			**FREE**

WR Welcome Reception
EL Exhibit Hall Buffet Lunch (Tuesday & Wednesday)
TS Technical Sessions
EX Exhibits
PR Proceedings *(includes Book and CD-ROM)*

#1 Subtotal Symposium Registration $__________

Foundation Contribution

❑ IMAPS Educational Foundation Contribution $__________

#2 Foundation Contribution $__________

Professional Development Courses

	✓	Course Title	Advance On/before 9/4	On-site After 9/4
S1		Hands-on Workshop (Wirebonding)	$900	N/A
S2		Hands-on Workshop (Screen Printing)	$900	N/A
S3		Hands-on Workshop (Soldering)	$900	N/A
S4		Lead-Free Solders – Tech/Apps (1/2 Day)	$500	$550
S5		Solder Joint Reliability (1/2 Day)	$550	$600
S6		Adhesion Science & Technology	$500	$550
S7		Advanced Materials for Microelect...	$550	$600
S8		Surface Mount Technology....	$500	$550
S9		Physics-of-Failure Based App.....	$500	$550
S10		RF/Microwave Hybrids; Principles.....	$500	$550
S11		Practical Methods to Design-In and.....	$500	$550
M1		Wire Bonding in Microelectronics	$575	$625
M2		Metal Plating for Electronics	$550	$600
M3		Technology of Screen Printing	$500	$550
M4		Microvias and Embedded Passives	$500	$550
M5		The Greening of Microcircuitry (1/2 Day)	$500	$550
M6		Fundamentals of Hybrid Microelectronics	$575	$625
M7		Advanced Organic Substrate Package......	$500	$550
M8		Failure Analysis of Hybrid Microelect.....	$575	$625
M9		Critical Materials Factors in High Perf....	$600	$650
M10		Fundamentals of Fabrication & Packaging...	$500	$550
M11		Area Array Technology - Processes.....	$500	$550
M12		Integrated Circuit Packaging & Assembly...	$575	$625
M13		Microelectronic Systems Pkg. (1/2 Day)	Students Only - Free	

#3 Subtotal PDC Registration $__________

Additional Purchases

❑ 10'x10' Exhibit Space
$1800 members, $2300 non-members

No. of Booths _____@ $ __________ Total $ __________
Company Name ______________________________

❑ Extra *IMAPS 2001 Proceedings (Book or CD-ROM)*
Book: $125 members, $200 non-members*
CD: $75 members, $150 non-members*
*(*Nonmember price includes 1 year IMAPS membership)*

❑ Book Version Qty. _____ $ ________
❑ CD-ROM Version Qty. _____ $ ________

(All publications add $7 to ship U.S.; overseas add $25)

#4 Subtotal Additional Purchases $__________

exhibitors

See the IMAPS on-line tradeshow at www.imaps2001.org

(as of April 27, 2001)

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Advanced Chemical
AI Technology, Inc.
AIM, Inc.
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Call for Abstracts

Abstract Deadline: September 14, 2001

HD International 2002

International Conference and Exhibition on High-Density Interconnect & Systems Packaging

IMAPS/CMP is seeking previously unpublished papers on recent works on the topics below.
Please send your 250-300 word abstract **electronically by September 14, 2001**, using the On-line submittal form at:
www.imaps.org/abstracts.htm
For questions, send email to: abstracts@imaps.org

Systems Packaging

Systems Applications
Portable OEM, Servers/Routers, Datacenter, Telecom, Medical, Space, Wireless, Automotive

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Power, HVAC, UPS, Back-up Power

Electrical Design
Signal, Power Distribution

Electronic Enclosures
Racks, Sheet Metal Cabinets, Plastics Impact on Design

Harsh Environmental Design
Automotive, Defense, Space, COTS

Industrial Design
Human Factors, Rapid Prototyping

Interconnect Technology
Connectors, Sockets, Cabling

Regulatory Compliance
Safety, Acoustics, EMI/EMC Design, Pollution

Shock and Vibration

Thermal Management
Fans/Air Movers, Heat Sinks, Thermoelectrics, Heat Pipes, Liquid Cooling, Refrigeration, Heat Exchangers, Heat Spreaders

High Density Packaging

HDP Applications
Computers, Portable/Wireless, Consumer, Automotive, Military, Telecomm, LAN Networks

Design and Test
Substrates, Assemblies, RF/Wireless, Chip/Substrate Wiring, Tradeoffs, Wafer Probe, AOI

High Density Substrate
Processing/Flex, Via Formation, Metallization, Lithography/Patterning, Process Integration, Bumping, Redistribution

Chip-Scale and Area Array Packages
Package Types, Applications

Known Good Die/Assemblies
Supply Strategies, Testing, Trends

Integrated Passives
Capacitors, Resistors, Inductors, Design Systems, Performance, Substrates

3D Packaging
Memory Arrays, Multiprocessors, System on Package (SOP)

Packaging Materials
Organic Dielectrics, Ceramic Dielectrics, Encapsulants, Substrates, Metals, Underfills

High Density Interfaces
Chip to Module (Wire Bond, Flip Chip), Module to Board (BGA, Flex) Common, Stacked Chips

Industry Issues

Markets and Infrastructure
Economic Studies, Market Trends, Technology Trends, Manufacturing Initiatives

Modeling, Analysis and Experimentation Techniques
Power/Signal Integrity, Thermal, Stress, Electrical Performance, Power Cycling

Electrical Modeling/Simulation
Concurrent Design & Analysis

Emerging Technologies
Superconductors, Exotic Substrates, Optical Interconnects, MEMS

Reliability
Capacitors, Resistors, Inductors, Design Systems, Performance, Failure Analysis, Defect Mechanisms

Design/Software Tools
Bumping and Redistribution Processes, Assembly, CFD, CAD, CAE, EDA

IMAPS/CMP is seeking previously unpublished papers on recent works on the above topics. Please send your 250-300 word abstract ***electronically by September 14, 2001****, using the On-line submittal form at:*
www.imaps.org/abstracts.htm
Mail/Fax is not encouraged.

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IMAPS V.P. of Technology:
R. Wayne Johnson, Auburn University

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Register for these events on page 32

Microelectronics Marketing Research Council (MMRC)

Fall Meeting

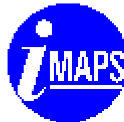
Optoelectronics Packaging:
Issues, Enabling Technology, and Government Policy Considerations
Westin Fairfax Hotel
Washington, DC
October 5-7, 2001

Co-sponsored by:
IMAPS & MMRC

Program Chair: E. Jan Vardaman, TechSearch International Inc.

This MMRC meeting will focus on optoelectronics packaging. Presentations focus on the market for this exciting technology, including drivers for the growth of the optoelectronics industry. Key roadmaps from around the globe are presented. Issues such as requirements for low-cost packaging solutions, material and substrate needs, assembly equipment automation requirements enabling the mass production of low-cost packages are addressed. Key U.S. Government funding activities and policies to promote the development of the optoelectronics industry are addressed by a group of distinguished presenters. Bus service provided to Baltimore, see page 32.

Registration is extremely limited! Register now!



IMAPS Advanced Technology Workshop on Optoelectronics

Radisson Hotel Bethlehem
Bethlehem, PA
October 11-14, 2001

General Chair: Tom Green, *tgreen@northampton.edu*
NTCμ, Northampton Community College

Technical Chair: Bill Heffner, *wheffner@agere.com*
Agere Systems (*formerly Lucent Optoelectronics*)

An optoelectronics packaging ATW is planned for October 11-14 in historic Bethlehem, Pennsylvania, located about 2.5 hours north of the BWI airport. The optoelectronics component industry has enjoyed a period of unprecedented growth spurred on by the insatiable desire for higher data rate transmission and increased bandwidth. This ATW will bring together scientists and engineers from industry, academia and government to address the unique technical challenges faced by all in the optoelectronic packaging arena. The workshop follows on the heels of the IMAPS National show with a Thursday night kick off and Keynote address by John Pittman of Agere Systems. Friday's session addresses the packaging challenges posed by the various device types, e.g., detectors, modulators, amplifiers, MEMS, etc., along with their associated packaging processes. Saturday's sessions are all about alignment and automation issues. The evening session will be held across the river on the scenic campus of Lehigh University, where the focus will redirect to attachment and materials issues in opto packages. Sunday morning will include a buffet breakfast and a final wrap-up session. One of the ATW's highlights will be "The new kids in town." With a multitude of start-ups in the area we'll have the chance to interact and learn first hand some of the unique packaging issues and challenges facing new start-up companies.

Plenty of social time is planned to facilitate informal interaction among attendees. You'll have the chance to develop personal acquaintances as together we exchange views and share ideas on common problems. It's a historic event you don't want to miss! Bus service provided to and from Bethlehem, PA, see page 32.

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MAP OF DOWNTOWN BALTIMORE TO INCLUDE HOTELS!

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Thanks!

Things To Do In And Around Baltimore

Baltimore Area Convention And Visitors Association
http://www.baltimore.org

Baltimore MarketPlace
http://www.markpoint.com

My Baltimore
http://www.mybaltimore.net

Fort McHenry National Monument and Historic Shrine
http://www.nps.gov/fomc/index.htm

National Aquarium in Baltimore
http://www.aqua.org

Babe Ruth Museum
http://www.baberuthmuseum.com

Baltimore Museum of Industry
http://www.charm.net/~bmi/

Maryland Science Center
http://www.mdsci.org

Edgar Allen Poe House
http://www.digitalcity.com/baltimore/arts/venue.dci?vid=23317

B&O Railroad Museum
http://www.borail.org

Historical Electronics Museum
http://users.erols.com/radarmus/

U.S. Naval Academy
http://www.digitalcity.com/baltimore/arts/venue.dci?vid=49207

Baltimore Orioles
http://orioles.mlb.com

Baltimore Ravens
http://www.ravenszone.net/

Baltimore Sun On-Line
http://www.sunspot.net

Guide to Washington D.C.
http://www.washdc.org/

2001 Washington DC Guide
http://www.2001cityguides.com/washington-dc/index.htm

See You Next Year in Denver, Colorado • September 4-6, 2002

program

AT A GLANCE

Sunday October 7

8 AM - 4 PM
Registration Open

9 AM - Noon
Professional Development Courses (S4)

9 AM - 5 PM
Professional Development Courses (S6-S11)

9 AM - 5 PM
Hands-on Workshops (S1-S3)

1 PM - 5 PM
Professional Development Courses (S5)

5 PM - 6 PM
PDC Reception

Monday October 8

8 AM - 5 PM
Registration Open

8 AM - 5 PM
Silent Auction

Golf Tournament

9 AM - Noon
Professional Development Course (M5)

9 AM - 5 PM
Professional Development Courses (M1-M4) and (M6-M12)

1 PM - 5 PM
Professional Development Courses (M13)

6:30 PM - 8 PM
Welcome Reception
(at the Hyatt Regency Baltimore)

Tuesday October 9

7 AM - 6 PM
Registration Open

8 AM - 9:40 AM
Plenary Session & Awards Ceremony

9 AM - 4:30 PM
Spouse/Guest Program

9:30 AM - 6 PM
Exhibits Open

9 AM - 11 AM
Student Booth Judging

10:10 AM - 11:25 AM
Technical Sessions (TA2, TA3)

10:10 AM - 11:50 AM
Technical Session (TA1, TA4)

9:30 AM - 6 PM
Silent Auction

11:30 AM - Noon
Annual Business Meeting
(No lunch included)

Noon - 2 PM
Lunch in the Exhibit Hall

2 PM - 3:20 PM
Special Session (TP6)
NSF & IMAPS Foundation

2 PM - 5:25 PM
Technical Sessions (TP1-TP5)

4 PM - 5:30 PM
Student/Industry Panel

4:30 PM - 6 PM
Octoberfest

5:30 PM - 6:30 PM
Student/Industry Reception

Wednesday October 10

7 AM - 5 PM
Registration Open

8 AM - 10:55 AM
Technical Sessions (WA1, WA3, WA4)

8 AM - 11:20 AM
Technical Sessions (WA2)

9 AM - 5 PM
Exhibits Open

9 AM - 4 PM
Silent Auction

9 AM - 5:30 PM
Spouse/Guest Program

Noon - 2 PM
Lunch in the Exhibit Hall

1 PM - 4 PM
Poster Session

2 PM - 5:25 PM
Technical Sessions (WP1-WP4)

Thursday October 11

7 AM - Noon
Registration Open

8 AM - 11:20 AM
Technical Sessions (THA1-THA4)

9 AM - Noon
Exhibits Open

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